LOW POWER NOVEL HYBRID ADDERS FOR DATAPATH CIRCUITS IN DSP PROCESSOR

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Abstract

A majority of the portable multimedia embedded devices like mobile phone, notebook computers which interfaces with information from the real-world environment are essentially Digital Signal Processing (DSP) circuits whose main building block is a Multiplier-Accumulator (MAC). The performance of the full adders that are a part of the MAC unit can significantly affect the efficiency of the whole system. Hence the reduction of power consumption in Full adder circuit is necessary for low power applications. In this paper, the various adder cell circuits are implemented using different CMOS logic structures and their performance is analyzed in 130nm technology. Further, two novel Full adder cells called HYBRID I and HYBRID II are proposed for data path circuit and simulated using 130nm technology with BSIM model. The Post layout is developed for these adders and its Performances like Power, Delay and Power-delay product-PDP are analyzed and compared with the other existing adders. These Hybrid Full adders show the better performance than other adders and operate at low voltage with good signal integrity, thereby making them suitable for high performance applications.

Keywords: Low power; MAC unit; full adder; dynamic power; Power Delay Product.

1. Introduction

Due to the rapid growth in portable electronics and communication systems like laptops, etc., the low power microelectronic devices have become very important in today world. In fact, Low-power VLSI chips have emerged as highly in demand for designing any subsytem. Moreover, Lower system power consumption is an essential for more applications than ever due to the dramatic increase in power-conscious applications. Low power circuit is realized using both hardware and software approach. Now a day, there is an increase in portable applications requiring small area, low-power and high- throughput circuitry [1]. Integrated Circuits(IC) devices are more advanced in computer science. In many VLSI applications, arithmetic operations are used extensively. Mostly the digital processing requires high speed and low power multiplier accumulator (MAC) unit. The addition and multiplication are the important operation in this unit. Specifically, speed and power efficient implementations of a adders are a very challenging problem. With the increase in complexity of VLSI systems and amount of power available in certain systems like cell phones and digital cameras, minimizing power consumption is essential. Lowering power consumption not only increases reliability, but also leads to save the package costs due to reduced heat dissipation. The main contributor to overall power dissipation in CMOS VLSI circuits is dynamic power consumption which accounts for up to 80% of the total power [1]. The dominant source of power dissipation is the dynamic power dissipation due to the charging and discharging of the node capacitances and is given by:

$$P=0.5\ CV_{dd}^{2}\ E\ (sw)\ f_{clk} \qquad (1)$$

where C is the physical capacitance of the circuit, V_{dd} is the supply voltage, E(sw) (switching activity) is the average number of transitions in the circuit per $1/f_{clk}$ time, and f_{clk} is the clock frequency. In order to reduce the power consumption of the adders any one of the above factors of circuit to be reduced. In this work different logic structure is used for constructing the adders for low power DSP application.

This paper is organized as follows: the full adder cell for MAC unit is described in the section II, operation of exciting few full adders are described in the section III, proposed new two Hybrid adders are given in section IV, simulation results and discussion are presented in the section V and finally conclusion is given in the section VI.

2. Full Adder Cell

Generally, a full adder is defined as a logical cell that performs an addition operation on three one-bit binary numbers. The full adder produces a two-bit output which is carry and Sum .Full Adder cell is implemented in low power and high performance data path circuit.The full adder consist of three input signals, i.e., A, B, and C (carry in), and two output signals sum and carryout which is shown in Fig. 1.

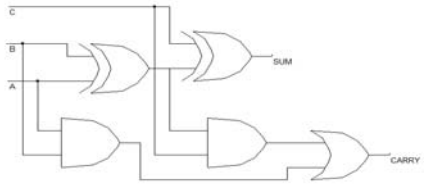


Fig.1 . Full Adder cell

The basic operation of full adder is given by the standard Boolean expressions as,

$$C = AB + BC + CA \quad (2)$$

$$S = ABC + A'B'C + AB'C' + A'BC' \quad (3)$$

There are various design techniques for implementation of full adder circuit is available. Some of them are Multiplexing Control Input Technique (MCIT), Gate Diffusion Input technique (GDI), Technique based on static CMOS Inverter, Multi-threshold CMOS circuit technique (MTCMOS)[4-9]. The existing Shannon based full-adder cell has been executed for the sum operation and the carry operation separately. Both sum and carry circuits are combined based on Shannon theorem, as modified Shannon. This has the demerits of more number of transistors, high power consumption, and large area requirement and pass transistor logic threshold voltage loss problem. In order to overcome the drawback of existing full adder circuits, the proposed full adder circuits has been implemented. In the proposed full adder cell, Pass transistor logic is utilized among all the other logic styles available as it is found to enhance the circuit performance in terms of speed, power and transistor counts. The adder cell can be applied to implement low power and high performance data path circuits.

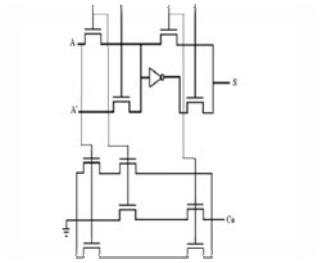
In this paper, different full adder circuits Shannon Based Full Adder, Modified Shannon, Transmission Function Full Adder TFA, Full adder using 14T, Full adder using 10T, Full Adder Using Majority Function and Full Adder Using Not Gate FA[8-9] are simulated and analyzed the performance using the software tool HSPICE with technology 130nm. 130nm is the most economic technology for stand-alone radio chips and other devices that combine RF and wired high-speed interface functions with a small amount of digital logic. New two Hybrid FAs are implemented using 14T and Shannon FA. The main features are High-speed and high-resolution, ultra low power, robust performance, immunity to noise & manufacturing variations.

3. Existing Full Adders

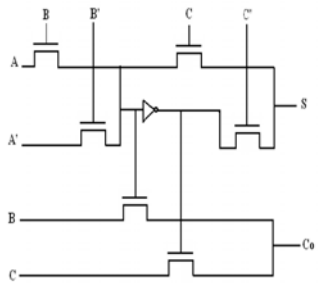
Adders are the basic building module in all multipliers, filters and MAC unit of DSP processor. So employing fast adders plays a key role in the performance of the entire all data path circuits. In this section different adder cells are described and analyzed. They are Shannon Based Full Adder, Modified Shannon, Transmission Function Full Adder TFA, Full adder using 14T, Full adder using 10T, Full Adder Using Majority Function and Full Adder Using Not Gate FA [6-9].

The existing full adder was designed with the help of MCIT for a full adder circuit and Shannon based adder using pass transistor logic constructed by combining the MCIT technique for sum and Shannon operation for carry. An input B and B’ are used as the control signal of the sum circuit (Fig. 2. a). The carry

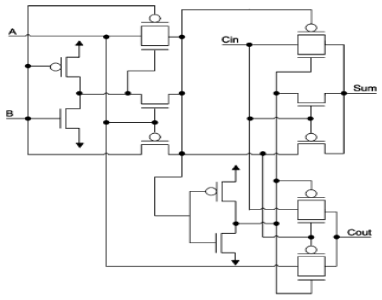
circuit is designed using the Shannon complementary pass transistor logic, and uses only the inputs A, B and C [8].In Shannon adder, the A, B and C along the with their complements are the inputs. B and B' are used as control signal of the sum circuit. C and C' are the differential nodes of the circuit .Sum and carry are the outputs. It has 12 transistors. In this circuit,all the pass inputs are connected to VDD line so that the pass gates are always ON.



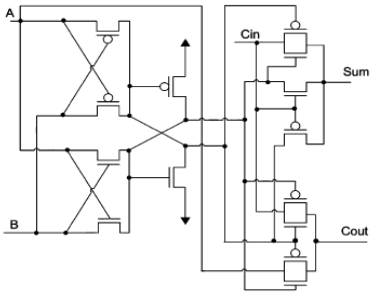
(a)Shannon adder



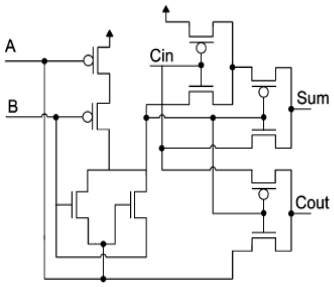
(b) Modified Shannon



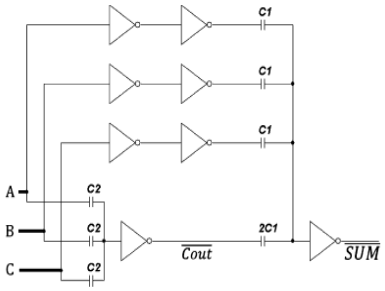
(c) Transmission Function Full Adder



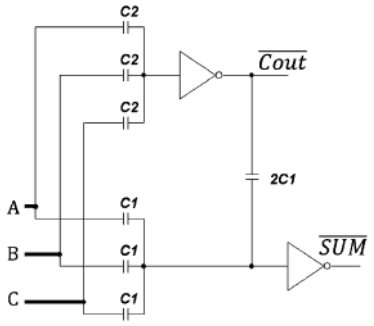
(d) Full Adder Using 14T



(e) Full Adder Using 10T



(f) Full Adder Using Not Gate



(g)Majority Function-Based Full Adder

Fig. 2. Different Full adder circuits

In the shannon full adder cell the sum and carry are executed separately and waveforms are also obtained. Now the shannon sum and carry are combined as Shannon. By using Shannon's theorem the sum and the carry expressions are condensed and thereby the transistor count has decreased [7]. In the existing design of full adder the carry is generated using six transistors where as the modified Shannon full Adder [9] design uses only two transistors. Thus the total chip area gets reduced. Therefore the power has also minimized to a considerable amount. (Fig .2. b). The advantage of the Modified shannon are less number of transistors, and better voltage swing.

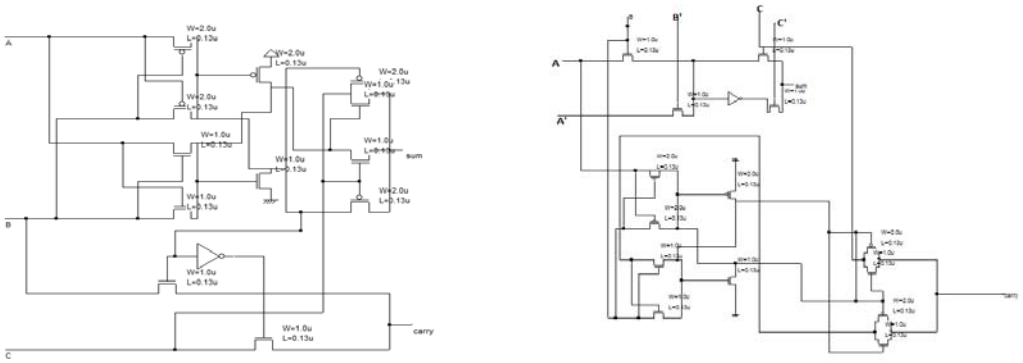
Transmission Function Full Adder (TFA) is another important of the full adder implementation techniques, which is shown Fig. 2. c. Based on transmission function theory, the circuit is implemented. It has 16 transistors, A, B and C are the inputs and sum and Carry and it requires double the number of transistors to design the function. It has low power consumption and this is good for designing use of XOR or

XNOR gates. The main drawback of this circuit is that it lacks in driving capability, more number of transistors are needed. It also have lower loading of the inputs and intermediate nodes, low number of transistor count and balanced generation of Sum and Carry signals, Fig. 2.d shows the Full adder using 14T use more than one logic style for the implementation and is called as a mixed logic design style. The number of transistors required is 14,and circuit has 3 inputs and 2 outputs,[9] Full adder using 14T generates A⊕B and use it along with its complement as a select signal to generate the output of the circuit. The advantage of 14T is small transistor count and enhances the non full swing pass transistor. The main drawback is that produce high capacitance values for the input signals.

Full adder using 10T use more than one logic structure for the implementation and is called as mixed logic design structure. The numbers of transistors required to implement this circuit is 10 and A, B and Cin are the inputs. Sum and Carry are the outputs. The demerits of this circuit is that produces high capacitance values for the inputs This full adder lack driving capabilities in fan-out situation and also the performance degrades drastically when 10T and 14T are cascaded[7-9]. Complement of Sum is implemented using five input Majority NOT function(see Fig. 2 .f) . Two capacitors that are connected to the complement of Cout are parallel. Therefore,the capacitances of them are added. Each successive couple inverter gates on top of the figure provide A,B and C inputs for the five-input Majority NOT function. The outputs of the circuit are obtained as the complements of Sum and Cout The Fig. 2. g shows the Majority Function based FA is simple logic circuit that performs as a majority vote to dertermine the output of the circuit.This function of the circuit has only odd numbers of input and its output is equal to one when the number of inputs one is more than zero.It requires very less number transistor,but the output depends on the capacitance of the input circuit. In order to overcome the drawbacks of existing adders two Hybrid adders are proposed, which are given in next section.

4. Proposed HYBRID Adder for MAC Unit

The Multiply Accumulate unit- MAC consist of basic Full adder cell. Based on the merits and demerits of the existing adder's features, the new Hybrid Full adders are designed. Here, seven existing full adders are modeled using 130nm technology with BSIM. These full adder circuits are analyzed for all the eight combinations of binary inputs with voltage scaling technique (at various supply voltages). From the analyzed circuits, it is found that 14T and Modified Shannon has better the functionality than the other existing circuits. Using 14T and Shannon Modified adders, new two hybrid adders are designed. The combination of 14T's Sum and Modified Shannon's carry is implemented, called as Hybrid-I, which is shown in Fig. 3.a .Sum circuit is built using 14T adder and carry is used with Modified Shannon Full Adder, The width is optimized by transistor sizing to bring the better power consumption without degrading the delay. The combination of 14T's Carry and Modified Shannon's Sum is implemented, named as Hybrid-II which is shown in Fig.3.b. Hybrid I and Hybrid II circuits consist of 14 & 16 transistors respectively. The optimal value of power is obtained by changing the size of the transistor (W/L) and the operating supply voltage Vdd. The width of the PMOS and NMOS transistors are alerted from 2.0 µm to 0.15 µm for optimizing Power Delay Product (PDP). These circuits provide good driving capability and better power delay performance.



a. Hybrid-I Full adder b. Hybrid-II Full adder

Fig .3 Novel Hybrid Adders

5. Results and Discussion

All adder circuits are implemented and simulated using HSPICE with model 130nm technology for which parasitic capacitance are considered in the result. A proper simulation test bench is used to simulate a real

environment and minimum output load is used for power and delay measurements. Seven existing adders and the two new Hybrid adders are simulated and their layouts are developed. The circuit performances are studied using voltage scaling technique (3V, 2V & 1v). All full adder circuits are analyzed for all the eight combinations of binary input and also for various supply voltages. From the analyzed circuits, it is found that 14T and Modified Shannon satisfies the full adder combination giving the better performance. Therefore Hybrid I and Hybrid II circuits are developed using14T and modified Shannon full adder.

Table.1 shows the sum and carry voltage level for all the full adder circuits at Vdd =1V, 2V, and 3V.All the full adder circuits are compared at different voltages. The Full adder using Majority function has the lowest number of transistors with the count of 4. It is observed that the voltage loss is less for Hybrid I full adder circuits. Hybrid I full adder shows excellent voltage swing at sum and carry outputs. In Table.2: the power and delay for all the full adder circuits at Vdd=1V, 2V and 3V are given. Comparing the performances of the full adder circuits it is observed that the voltage loss is less for Hybrid-I sum, Hybrid-I has the lowest Delay and Modified Shannon has the lowest power consumption. Comparison of the power and delay of HYBRID I and HYBRID II Full adders with other seven adders are shown in Fig .5. All circuit simulations are carried out in 130nm with BSIM model using HSPICE. The power delay product at various Vdd of Hybrid adders are shown in Table.3.HYBRID I adder has very less PDP, which is shown in Fig.6.

Table 1. Sum And Carry voltage level Analysis of Different Full Adders at Vdd = 1V,2Vand 3V at 130nm Technology

S.no	Adder	No. of Transistor	Vdd 1V		Vdd 2 V		Vdd 3 V	
			sum (V)	carry(V)	sum (V)	carry(V)	sum (V)	Carry(V)
1.	TFA	16	0.96	0.6	1.7	1.9	2.5	2.9
2.	FA Using 10T	10	0.5	0.5	1.3	1.7	2.2	2.9
3.	FA Using 14T	14	0.98	0.96	1.84	1.96	2.6	2.9
4.	FA Using NOT GATE	16	0.98	0.5	1.83	1.2	3	2.5
5.	FA Using MAJORITY FUNCTION	4	0.7	0.7	1.9	1.7	3	3
6.	SHANNON ADDER	12	0.6	1	1.3	1.3	1.9	2.6
7.	MODIFIED SHANNON	8	0.6	0.3	1.6	1.7	2.6	2.7
8.	HYBRID-I	14	0.98	0.9	1.9	2	2.8	3
9.	HYBRID -II	16	0.6	0.9	1.3	1.9	1.9	2.9

Table 2. Power and Delay Analysis of Different Full Adders at Vdd =1V, 2V and 3V

S.no	Adder	VDD 1 V		VDD 2 V		VDD 3 V	
		power(w)	delay (ns)	power(w)	delay (ns)	power(w)	delay (ns)
1.	TFA	2.23E-06	10.04	2.68E-05	9.3	1.06E-04	9.12
2.	FA Using 10T	2.03E-07	24.67	4.63E-07	19.23	8.28E-07	6.39
3.	FA Using 14T	3.44E-06	9.19	6.16E-05	7.3	2.32E-04	6.39
4.	FA Using NOT GATE	2.52E-06	16.42	2.95E-05	7.3	1.14E-04	3.64
5.	FA Using MAJORITY FUNCTION	8.62E-07	6.38	1.25E-05	5.48	5.03E-05	4.56
6.	SHANNON ADDERS	1.08E-06	12.77	7.04E-06	7.3	1.98E-05	6.39
7.	MODIFIED SHANNON	6.05E-08	12.77	1.42E-07	13.68	1.88E-07	10.04
8.	HYBRID-I	1.26E-07	5.47	1.51E-06	3.64	6.08E-05	3.64
9.	HYBRID -II	2.49E-07	5.12	2.49E-06	5.48	9.1E-05	5.48

Table 3. Power Delay Product Analysis of Different 1 Bit Full Adder At Vdd =1V, 2V and 3V

Sno	Adder	Power delay product		
		VDD 1 V (e-15)	VDD 2 V (e-15)	VDD 3 V (e-15)
1.	TFA	2238	249.24	966.72
2.	FA Using 10T	5	8.9	5.21
3.	FA Using 14T	31.61	449.68	1482.49
4.	FA Using NOT GATE	41.37	215.35	495.49
5.	FA Using MAJORITY FUNCTION	5.49	68.5	229.36
6.	SHANNON ADDERS	13.79	51.39	126.32
7.	MODIFIED SHANNON	0.77	1.94	18.87
8.	HYBRID-I	0.68	5.49	221.31
9.	HYBRID -II	1.27	13.64	498.68

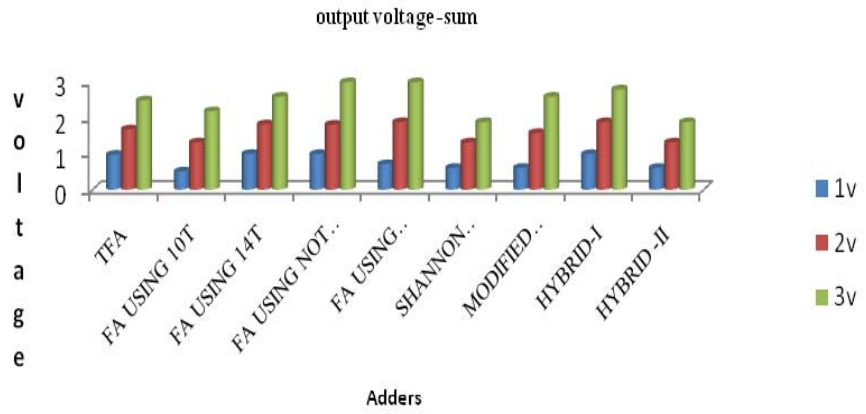


Fig. 4.a Sum output voltage for all adders

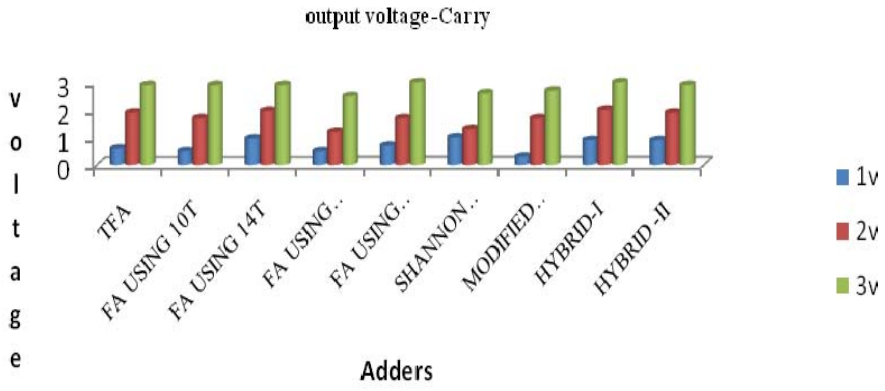


Fig. 4.b Carry output voltage for all adders

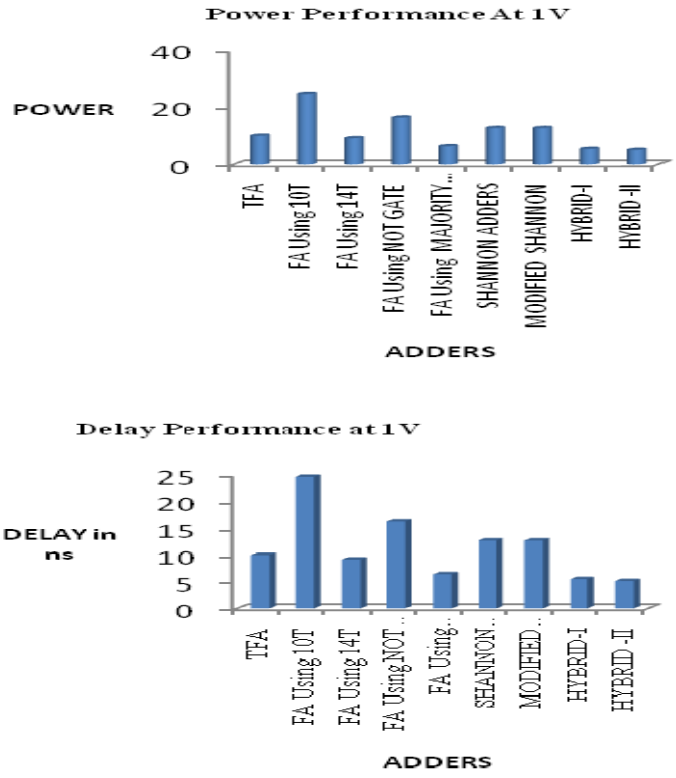


Fig. 5. Comparison of power and delay of Hybrid adders with other adder

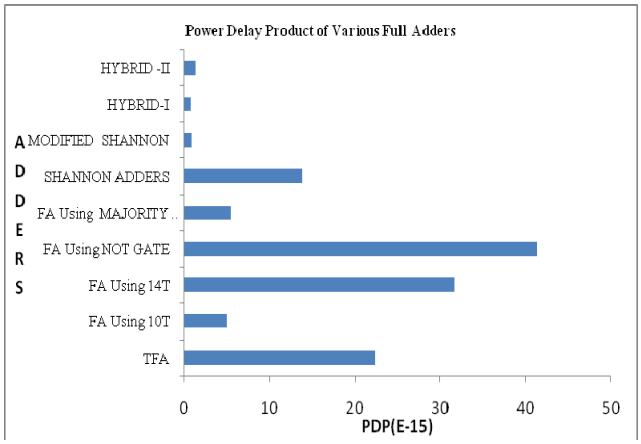


Fig. 6. Comparison of Power Delay Product of Hybrid adders with other adders

6. Conclusion

In this paper HYBRID I and HYBRID II full adders are proposed for data path circuit (MAC unit) for low power DSP application. The proposed circuit uses full adder using 14T and Modified Shannon circuits. The seven existing adders and two proposed full adder circuits are implemented and simulated in HSPICE using BSIM model at 130nm Technology .The power, voltage level, delay and PDP values of all the full adder circuits are analyzed. The optimal value of power and PDP is obtained by transistor sizing and voltage scaling. The performance analysis of various full adders at Vdd=1V, 2V, 3V using 130nm technology are carried out. It is observed from the simulated results that the proposed circuit has the lowest Delay, Voltage Loss and Power Consumption with area tradeoff. The functionality test of different full adders at Vdd=1V, 2V, 3V using 130nm technology are also verified. All 8 combinations of Binary input are tested for each circuit. It is found that HYBRID I has the best performance among all other full adder circuits. At low voltage level (Vdd=1), HYBRID I adder has very less power delay product (nearly 10-90% of improvement) compared with other adders. Here, all the circuits are simulated using the BSIM model at 130nm technology. This can also be tried for other models of technology less than 100nm.Therefore these Hybrid adders can be used for low power high performance circuits.

References

[1] Gray Yeap and Gilbert,(1998) Practical Low power Digital VLSI Design, Kluwer Academic Publishers.
[2] Rabaey.J,(2003) Digital Integrated Circuits: A Design Perspective, 2nd edition, Prentice-Hall.
[3] Pedram,(1996)Power Minimization in IC Design, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 1, pp. 3-56.
[4] Zhuang.N and Wu.H,(1992)A New Design of the CMOS Full Adder, IEEE J. Solid State Circuits, vol.27, no.5, pp.840-844,
[5] Sameer Goel, Ashok Kumar, and M.A.Bayoumi,(2006) Design of Robust Energy Efficient Full Adders for Deep Sub micrometer Design Using Hybrid -CMOS Logic Style", IEEE Trans. On VLSI Systems, vol.14, no.12.
[6] Wey K.C., Huang C.H and Chow H.C,(2002) "A New Low-Voltage CMOS 1-Bit Full Adder for High Performance Applications", IEEE, pp. 21- 24.
[7] Shalem R, John E, John L.K,(1999) A novel low-power energy recovery full adder cell, in: Proceedings of the Great Lakes Symposium on VLSI, pp. 380–383.
[8] Alioto M, Palumbo G, (2002) Analysis and comparison of the full adder block, IEEE Trans. VLSI 10 .pp806–823.
[9] Chang C.H, Gu J, Zhang M, (2005) A review of 0.18-µm full adder Performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integration System.vol. 13 ,pp 686-695.

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