

DESIGN OF MODULO-6-COUNTER USING CARBON NANOTUBE FIELD EFFECT TRANSISTOR

V.Saravanan¹ V.Kannan²

¹ Research Scholar, Sathyabama University, Tamilnadu , India

² Principal, Jeppiaar Institute of Technology, Tamilnadu, India.

¹vsaranmembra@yahoo.co.in

²drvkannan123@gmail.com

Abstract

In many digital applications like digital clock, frequency divider circuit and nano applications etc., designing of low power modulo counters is highly desirable. Designing of such a counters using existing technology i.e., CMOS technology has the limitations in-terms of power consumption, device scaling limitations and fabrications difficulties in nanometre range. This paper proposes the new design technique for modulo counters using the carbon nanotube field effect transistor (CNTFET). Counter performance is analyzed interms of speed and power consumption. This paper also analyses carbon nanotube (CNT) types, how the carbon nanotube is formed, and scaling limitations of the CMOS technology in nanometre range.

Keywords: Counters, CNTFET, Carbon Nanotube, CMOS, Nanometre.

1. Introduction

In many applications it is necessary to design the specific modulus counters by combining different modulus counter. For example mod-4 counter and mod-8 counter are combined to get mod-32 counter. Connection between the individual counter may be either asynchronous mode or synchronous mode, when these counters are designed for low power and nano applications, CMOS technology has limitations. In CMOS technology, Scaling of CMOS devices in the last few decades has increased the no of devices on chip to sustain any integrated circuits (ICs) as per Moore's law [Appenzeller J et al (2008) and Kurt A. Moen et al (2010)]. As per the Moore's law number of transistors fabricated on ICs is approximately doubled for every two years. When the scaling of existing technology i.e., CMOS technology is below 90 nm, it approaches scaling limit due to the increased short-channel effects, reduced gate control, exponentially rising leakage current[Radosavljevic M et al. (2003) and Davide Ponton(2009)]. Hence Research has started to explore novel materials and devices able to overcome or even replace the MOSFET based CMOS technology for future nano devices with in next decade before the CMOS technology reach its scaling limits. Many nano devices has been reported by the research groups, such as Carbon nanotube field effect transistor (CNTFET), resonant tunnelling diode (RTD), single electron transistor, and spinFET. Among these devices CNTFET is one of the best alternative to the today's MOSFET based CMOS technology due to their compatibility with high dielectric materials and near ballistic operation [Pecchia A et al. (2003)]. Due the scaling limit of the CMOS technology, designing of modulo counters for the nano applications using CMOS technology has limitations. This paper proposes the new design technique for designing the modulo counters to overcome the limitations of the CMOS technology.

The rest of this paper is organized as follows: Section 2 describes the Carbon Nanotube Based Transistor, Session 3 describes Design of CNTFET Based modulo-6 Counter; Session 4 describes the Simulation Results and Discussion. Session 5 Provides Conclusion.

2. Carbon Nanotube Based Transistor

Carbon nanotube is composed of one or more concentric layers of carbon atoms, single layer of graphite is called Single-walled carbon nanotubes (SWCNT) [Bachtold A, et al (2001), Li J, Zhang Q, Yan Y *et al.* (2007), and Kyung Ki Kim, et al (2011)] . Structure of graphene is shown in fig (1). Single-walled carbon nanotubes (SWCNT) are attractive for extreme scaling of integrated circuits due to their small diameters, long lengths and thermal stabilities. A SWCNT can be either semi-conducting or metallic. SWCNT are currently considered for application as transistors, diodes and interconnects in future integrated circuits, CNTs properties are strongly dependent on their chirality and diameter. The chirality is related to the angle of twist of the graphene sheet and can be described by the chiral vector. The chiral vector is a circular vector that is perpendicular to the axis of the tube. It is a linear combination of the base vectors a_1 and a_2 . In mathematical terms the chiral vector is defined by equation (1) [Chen Z, Appenzeller J, Lin Y-M *et al.* (2006), Rahman A, Jing Guo, Datta S and Lundstrom M S (2003)]:

$$C = na_1 + ma_2 \tag{1}$$

Where n and m are integers, which denotes the number of unit vectors along two directions in the honeycomb crystal lattice of graphene. Fig (2) shows the graphical representation of the chiral vector of (5, 0) zigzag single walled carbon nanotube on graphene.

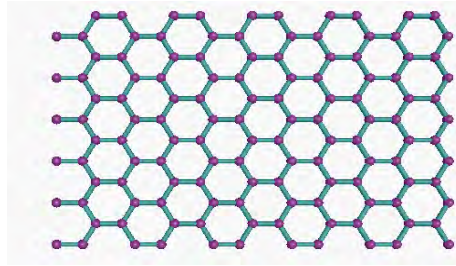


Fig (1) structure of grapheme

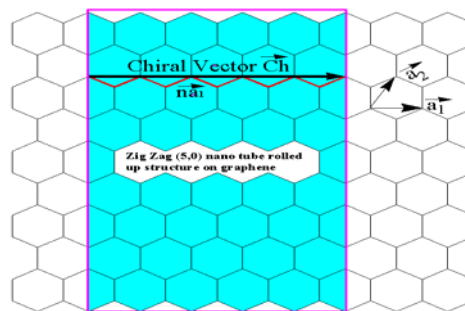


Fig. (2) Chiral vector of (5, 0) nanotube on graphene.

The electrical properties of carbon nanotubes are depends on their physical structure. Carbon nanotubes are three types depends on the (n, m) values: zigzag, armchair, and chrial. For a armchair tubes, $n = m$ and chiral angle (θ) is 30° . For example chiral vector $C = (5, 5)$ is the armchair nanotubes. For zigzag tubes, $m = 0$ and chiral angle (θ) is 0° . For example Chiral vector $C = (5, 0)$ is the zigzag nanotubes. For chiralNanotube chiral angle is $0^\circ < \theta < 30^\circ$. the chiral vector $C = (3, 2)$ is the chiral nanotube. Table 1 shows the types of carbon nanotubes and it's chiral vector [Khairul Alam, et al (2007), Han J, Jonker P (2002), Heinze S et al. (2002), Ian O'Connor, Junchen Liu, etal (2007), Raychowdhury A and Roy K et al (2005)].

A single-wall carbon nanotube (SWCNT) consists of one cylinder only and the Multi-wall carbon nanotube (MWCNT) consists of more than one CNT. Simple manufacturing process of this device makes it very promising replacement of MOSFET Technology. Fig (3) shows the schematic of the carbon nanotube based field effect transistor. In this CNT is used as channel between source and drain. Gate, length in the proposed model is 18nm. Except the gate region of the CNT, remaining part of the CNT is doped with n+ materials. High-k material is used as gate dielectric material with $k= 16$, with oxide thickness of 4nm. The current-voltage (I-V) characteristics of the CNTFET are similar to MOSFET's [Jie Deng, H.-S. Philip Wong (2007), J. Liu, et al (2007) , and Youngki Yoon, et al, (2008)].

Table.1. Types of carbon nanotubes

Types of SWCNT	Chiral Angle (θ)	Chiral vector (C_n)	Structure
Zigzag	0°	$(n,0)$, where $m=0$	
Armchair	30°	(n, n) , where $n=m$	
chiral	$0^\circ < \theta < 30^\circ$	(n, m)	mixture

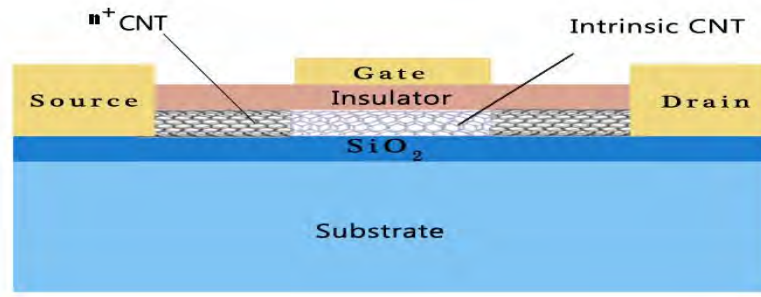


Fig (3) Schematic diagram of a carbon nanotube transistor

The drain to source current of the carbon nanotube field effect transistor is given by equation (2) [Deji Akinwande, et al (2008) Jie Deng, et al (2007) and Arijit Raychowdhury, et al (2004)].

$$I_{DS} = 2 \sum_{k_m}^M \sum_{k_l}^L [J_{m,l} (0, \Delta \Phi_B) - J_{m,l} (V_{ch,DS}, \Delta \Phi_B)] \quad (2)$$

Where M and L are the sub-bands and sub-states respectively. $V_{ch,DS}$ is the Fermi level difference within the channel. $J_{m,l}$ is the sub-states current. Fig (4) shows the device current characteristics for both CNTFET and MOSFET. For this simulation carbon nanotube FET gate length is 18nm and MOSFET it is 180nm. CNTFET shows the better performance in terms of high on-state current, high speed and high linearity.

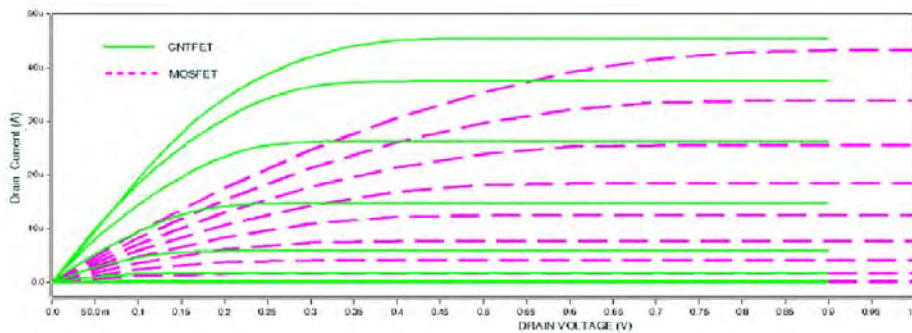


Fig (4) Characteristics of CNTFET and MOSFET

3. Design of CNTFET Based Modulo-6-Counter

In this paper design of Modulo-6-counter using carbon nanotube field effect transistor (CNTFET) is presented. It counts binary word from 0 to 5. Table 2 shows the counting sequence of modulo-6 counter. Counter has to count maximum of six pulses. Hence it requires three flip flops (TFF0-TFF2). First flip flop toggles (q_0) on each clock pulse, so the logic equation for its T input is given by equation (3)

$$T_0 = 1 \quad (3)$$

This can be implemented by connecting T input to constant HIGH level. Second flip flop toggles (q_1) next clock pulse when $q_0=1$ and $q_2=0$, Input T_1 for this logic function is given by following logic equation (4).

$$T_1 = q_0 \overline{q_2} \quad (4)$$

The above equation can be implemented by ANDing q_0 , $\overline{q_2}$ and connecting gate output to the Input T_1 . Third flip flop toggles (q_2) next clock pulse when $q_0 = 1$, $q_1 = 1$ and $q_0=1$, $q_2=1$, hence the logic input equation for T_2 input given by (5). By combining all logic equations (3)-(5), logic diagram of modulo-6-counter is obtained. which is shown in fig (5)

$$T_2 = q_0 q_1 + q_0 q_2 \quad (5)$$

Table-2: Counting sequence of modulo-6- counter

Clock Pulse	q ₂	q ₁	q ₀
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	0	0	0
8	0	0	1

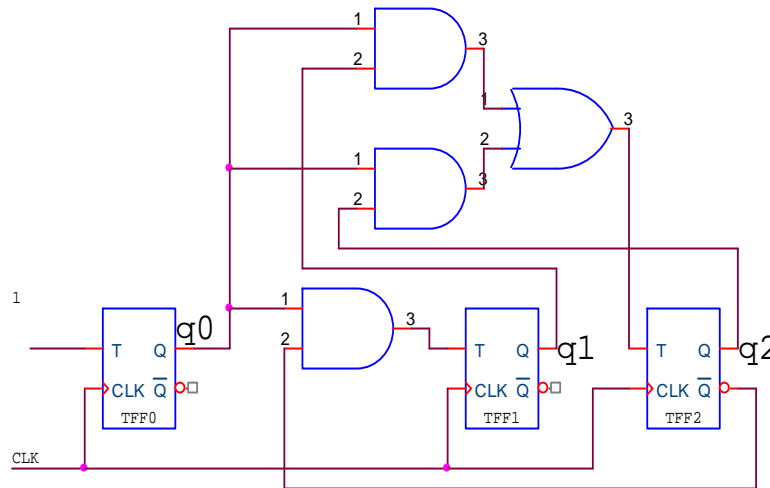


Fig (5) Modulo-6-counter

4. Simulation Results and Discussion

Fig (6) shows the simulation results of modulo-6- counter. From the results, its counting sequence is as follows: 000,001,010,011,100,101,000,001 and so on, Hence it counts only 0 to 5. Thus the counter acting as modulo-6-counter. Design and simulation is done using both CMOS and CNTFET Technology. Propagation delay of CNTFET based design is 2.5ns where as for CMOS based design is 37.4ns Fig (7) shows the propagation delay Comparison of CNTFET and CMOS technology. Power consumption of CNTFET based design is 0.21μw and for CMOS based design is 1.37μw, Power Comparison of Modulo-6-counter for CNTFET and CMOS technology is shown in fig (8)

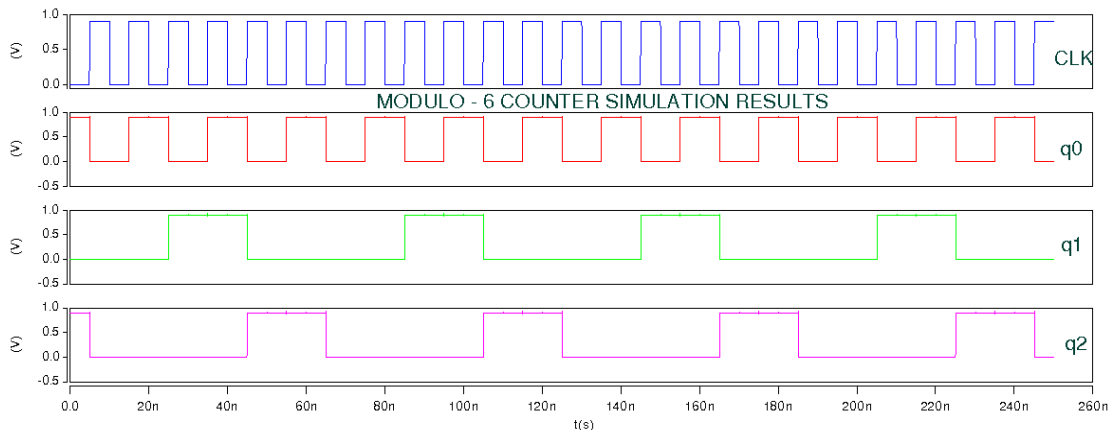


Fig (6) Simulation results of Modulo-6-counter

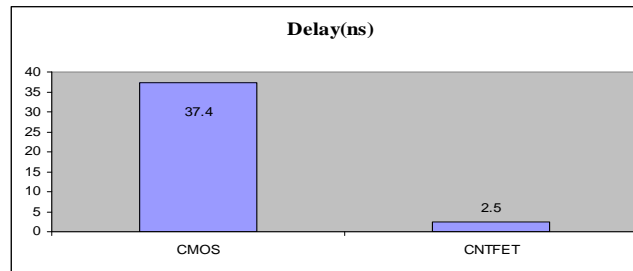


Fig (7) Delay comparison of Modulo-6-counter

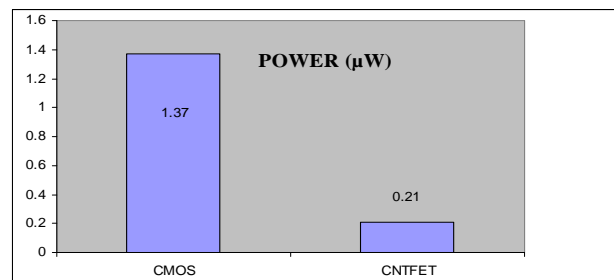


Fig (8) Power comparison of Modulo-6-counter

5. Conclusion

The new design of Modulo-6-counter using carbon nanotube field effect transistor (CNTFET) is presented. The performance of proposed design is better in terms of power consumption and delay than CMOS Technology. Hence the proposed counter design can be used in digital clock, frequency divider circuit and nano applications etc., Threshold voltage of the CNTFET can be easily controlled by changing the chirality vector of the CNTs, digital circuit can be designed for the required threshold voltage. Performance of CNTFET in current conduction is high due to their high gate capacitance; this high capacitance value increases the ON state current of the device, Gate capacitance value is increased by using high-k dielectric material as gate dielectric. Since CNTFET can be fabricated on the small chip area, this device will be the best replacement for the MOSFET based digital circuit.

References:

- [1] Appenzeller J et al (2008), "Carbon Nanotubes for High-Performance Electronics Progress and Prospect", *Proceedings of the IEEE*, Vol. 96, No. 2, pp. 201-211.
- [2] Kurt A. Moen et al (2010), "Evaluating the Influence of Various Body-Contacting Schemes on Single Event Transients in 45-nm SOI CMOS" *IEEE Transactions on Nuclear Science*, Vol. 57, No. 6, pp 3366 – 3372
- [3] Davide Ponton (2009) "Design of Ultra-Wideband Low-Noise Amplifiers in 45-nm MOS Technology: Comparison Between Planar Bulk and SOI FinFET Devices", *IEEE Transactions on Circuits and Systems*, Vol. 56, No. 5, pp 920 – 932.
- [4] Radosavljevic M et al. (2003), "Drain Voltage Scaling in Carbon Nanotube Transistors" *Appl. Phys. Lett.*, Vol. 83, No. 12, p. 2435-2437.
- [5] Pecchia A et al. (2003), "Electronic Transport Properties of Molecular Devices", *Physical Review Letters*, Vol. 19, pp. 139-144.
- [6] Kyung Ki Kim, Yong-Bin Kim, Ken Choi (2011), "Hybrid CMOS and CNFET Power Gating in Ultralow Voltage Design" *IEEE Transactions on Nanotechnology*, Vol. 10, No. 6, Pp 1439-1448
- [7] Li J, Zhang Q, Yan Y et al. (2007), "Fabrication of Carbon Nanotube Field-Effect Transistors by Fluidic Alignment Technique", *IEEE Transactions on Nano-Technology*, Vol. 6, No. 4, pp. 481-484.
- [8] Bachtold A, Hadley P, Nakanishi T and Dekker (2001), "Logic Circuits with Carbon Nanotube Transistors", *Science*, Vol. 294, No. 9, pp. 1317-1320
- [9] Chen Z, Appenzeller J, Lin Y-M et al. (2006), "An Integrated Logic Circuit Assembled on a Single Carbon Nanotube", *Science*, Vol. 311, No. 5768, p. 1735.
- [10] Rahman A, Jing Guo, Datta S and Lundstrom M S (2003), "Theory of Ballistic Nanotransistors", *IEEE Transactions on Electron Devices*, Vol. 50, No. 10, pp. 1853-1864
- [11] Raychowdhury A and Roy K (2005), "Carbon Nanotube-Based Voltage-Mode Multiple-Valued Logic Design", *IEEE Trans. Nanotechnology*, Vol. 4, No. 2, pp. 168-179.
- [12] Han J and Jonker P (2002), "A System Architecture Solution for Unreliable Nanoelectronic Devices", *IEEE Trans. Nanotechnology*, Vol. 1, pp. 201-208.
- [13] Heinze S et al. (2002), "Carbon Nanotubes as Schottky Barrier Transistors", *Physical Review Letters*, Vol. 89.
- [14] Ian O'Connor, Junchen Liu, et al (2007) "CNTFET Modeling and Reconfigurable Logic-Circuit Design" *IEEE Transactions on Circuits and Systems*, Vol. 54, No. 11, pp 2365-2379
- [15] Khairul Alam, Roger Lake, I (2007) "Role of Doping in Carbon Nanotube Transistors With Source/Drain Underlaps" *IEEE Transactions on Nanotechnology*, Vol. 6,
- [16] Youngki Yoon, James Fodor, and Jing Guo, (2008) "A Computational Study of Vertical Partial-Gate Carbon-Nanotube FETs" *IEEE Transactions on Electron Devices*, Vol. 55, No. 1.
- [17] J. Liu, I. O'Connor, D. Navarro, F. Gaffiot (2007) "Design of a Novel CNTFET-based Reconfigurable Logic Gate" *IEEE Computer Society Annual Symposium on VLSI (ISVLSI'07)*

- [18] Jie Deng, H.-S. Philip Wong (2007) "A Compact SPICE Model for Carbon- Nanotube Field-Effect Transistors Including Nonidealities and Its Application Model of the Intrinsic Channel Region" IEEE Transactions on Electron Devices, Vol. 54, No. 12, Pp 3186-3194
- [19] Deji Akinwande, Yoshio Nishi, and H.-S. Philip Wong, (2008) " An Analytical Derivation of the Density of States, Effective Mass, and Carrier Density for Achiral Carbon Nanotubes" IEEE Transactions On Electron Devices, Vol. 55, No. 1, Pp 289 – 297
- [20] Jie Deng, H.-S. Philip Wong, (2007) "A Compact SPICE Model for Carbon- Nanotube Field-Effect Transistors Including Nonidealities and Its Application " IEEE Transactions On Electron Devices, Vol. 54, No. 12, Pp 3195 – 3205
- [21] Arijit Raychowdhury, Saibal Mukhopadhyay, and Kaushik Roy (2004) "Circuit- Compatible Model of Ballistic Carbon Nanotube Field-Effect Transistors" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 23, No. 10, pp 1411 – 1420.



V. Saravanan was born in vellore, Tamil nadu, India in 1981. He received his bachelor degree in Electronics and communication Engineering from Ganadhipathy Tulsi's Engineering college, vellore, TamilNadu in the year 2004 ,ME in Applied Electronics from Sathyabama University, Chennai in the year 2007. He is presently a research scholar in the Department of Electronics and communication Engineering, Sathyabama University. He has 8 years of teaching experience. He is a life member of ISTE



Dr.V.Kannan was born in Ariyalore, Tamil nadu, India in 1970. He received his Bachelor Degree in Electronics and Communication Engineering from Madurai Kamarajar University in the year 1991, Masters Degree in Electronics and control from BITS, Pilani in the year 1996 and Ph.D., from Sathyabama University, Chennai, in the year 2006. His interested areas of research are Optoelectronic Devices, VLSI Design, Nano Electronics, Digital Signal Processing and Image Processing. He has 140 Research publications in National International Journals / Conferences to his credit. He has 20 years of experience in teaching and presently working as Principal of Jeppiaar Institute of Technology, Chennai, India, He is a life member of ISTE.