SPURIOUS POWER SUPPRESSION TECHNIQUE FOR VLSI ARCHITECTURE

R.SESHADRI M.E.,(Ph.D)
Research Scholar,
Anna University Chennai, Tamilnadu
seshadriaec@gmail.com.

Dr.S.RAMAKRISHNAN Ph.D
Research Supervisor / Professor & Head, Department of IT
Sakthi Mariamman Engineering College, Anna University Chennai
Sriperumbudhur, Kanchipuram - 602 105, Tamilnadu
jkang69@yahoo.com.

G.HEMALATHA
M.E Applied Electronics
Arunai Engineering College, Anna University Chennai
Tiruvannamalai-603, Tamilnadu
Hemalatha821990@gmail.com

V.VIJAYALAKSHMI
M.E.Applied Electronics
Arunai Engineering College, Anna University Chennai
Tiruvannamalai-603, Tamilnadu
Viji5818@gmail.com.

Abstract

Using spurious power suppression technique (SPST) in VLSI will reduce the power consumption of the system significantly. Here we are going to implement this design in Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) filter architecture. When we are using this technique in this multipliers the no of partial products generated will be reduced to half which reduces the computation .Then obviously the power consumption is also reduced by this method using the Spartan 2 hardware device.

Keywords : SPST,FIR,IIR,Power dissipation, Partial products.

1.Introduction :

Minimized scaling Integrated circuits and their related researches are still finding solutions for further minimization .The reduced power, area and thermal dissipation is the goal for the VLSI researchers .There are different methods are used for the minimized sources with efficient performance. Here a method is discussed for the reduction of the power. In this paper the ultimate focus is on the power. The power reduction with the same performance as like in other technique is discussed here. The power dissipation in the integrated circuits is more because of the dynamic power dissipation. This is mainly because due the charging and discharging of the capacitance in the circuit.

The formula used for the calculation of the dynamic power dissipation is as follow

$$P_d = CLV^2F \qquad (1)$$

By reducing the capacitance, clock frequency ,power supply ,switching activity we can reduce the power consumption of the integrated circuits .Here by reducing the partial products generated in the repeated addition of the multipliers we can reduce half of the power consumption when compared to other multipliers. We can use the IIR and the FIR filters for this process. Here this technique is simulated using the FIR filter also.

Multipliers with high speed are essential of digital applications for example signal processing. Even in general purpose processors high speed multipliers are most required. In classic multipliers the multiplication process is the repeated addition operation. The multiplier is added repeatedly for the value of the multiplicand times .This is the long taking process. Since by using different techniques the design of the fast multipliers are most preferable nowadays. In order to avoid the accumulation of the partial products generated in the multiplication process the method followed here is known as the spurious power suppression technique (SPST)

.In this technique the given multiplicand is recoded using radix 4 modified booth algorithm. And the recoded reduced number of the multiplicand is considered for the multiplication process. The multiplication is performed by taking the two's compliment for the given multiplier term. This paper specifically deals with how could we implement this technique in the FIR and the IIR filter structure to function as the fast multiplier.

In the following content of the paper we are going to deals with (i) Spurious power suppression technique (ii)IIR filter and it's implementation.(iii)FIR filter and it's implementation. (iv)obtained results and finally the (vi)conclusion of this concept proposed.

2.Spurious power suppression technique (spst):

The SPST technique is basically depend on the radix 4 modified booth algorithm. It deals with the recoding of the given multiplicand and reduce the number of the intermediate stages in the multiplication operation which maintains the speed of the process at the same time the power consumed will be reduced.

2.1 Radix 4 Modified Booth Algorithm :

Normally in booth algorithm the partial products generated for the 16 X 16 bit multiplication is 17bits since its inefficient application. Therefore we switch to the radix 4 modified booth algorithm in which the partial products is not generated by the shifting. The three bit encoding technique i.e. Recoding procedure is used here in this algorithm(1).

The following are the steps involved :

A-multiplicand , B-multiplier.

- A-1=0 then put zero in the right side of LSB of multiplier.
- If the multiplier bits is odd then add a extra 1 bit on left side of MSB.
- By using the truth table the partial products are generated.
- These new partial product is generated, each partial products is added 2 bit left shifting in regular sequence.

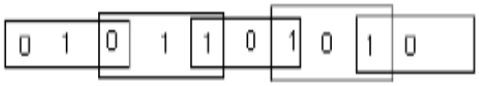

Fig.1.Grouping of the multiplier terms.

The figure.1 shows the pairing of the multiplier terms. The recoding is done depending on the grouping of the multiplier term. The zeros and ones in the multiplier term decides the recoding values of the grouped terms. Since the grouping is with three bits in each term the recoding value is generally allotted from 000 to the value 111. The following table shows recorded values for the grouped terms.

Example of the multiplication done with the above mentioned techniques is shown below. It will reduces inter multiplication steps to half that the operation to be performed is reduced to half for the same output. Since the speed is maintained as same for the normal operation even better performance is there. And also the power consumed is also reduced to the half. Since the power consumption is reduced the power dissipation in the form of the heat is also reduced .Therefore by this method the efficient architecture in any form is designed in VLSI.

Following Table will give the recoded values for the paired groups. This values were allocation is based on the Radix 4 Modified Booth Algorithm. The structure of the filters used and the calculations are given in following sections.

Block	Re-coded digit	Operation on X
000	+0	0A
001	+1	+1A
010	+1	+1A
011	+2	+2A
100	-2	-2A
101	-1	-1A
110	-1	-1A
111	0	0A

Table.1.Recoded values for modified booth algorithm.

Structure of IIR and FIR filters:

The following figure shows the structure of the third order IIR filter structure .It contains the delay elements and multiplier in it. The input and output relationship of the system is given by the following equations. The 16 bit data coefficient is given as input to the system. Then Each data elements to the delay unit .If L is the word length of the data then the data will be delayed by L times.

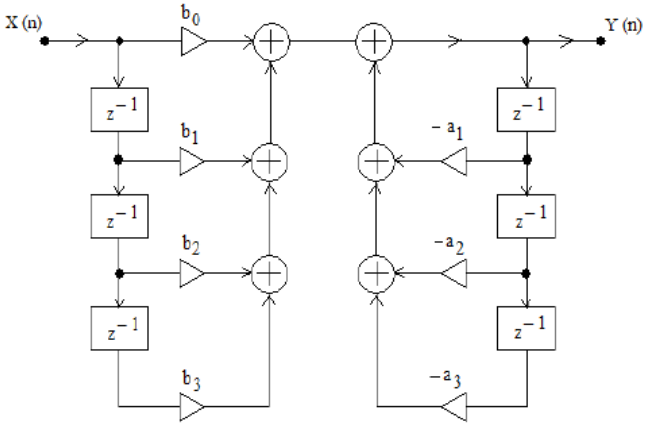

Fig.2.Structure of the IIR Filter.

The input and output relationship of the system is given by the following equation(2).The Z Transform of the system is also given by the equation(3).

$Y(n)=b_0x(n)+ b_1x(n-1)+b_2x(n-2)+b_3x(n-3)-a_1Y(n-1)-a_2Y(n-2)+a_3y(n-3)$ (2)

Z-transform of the given 3rd order difference equation and simplifying we get transfer function as:

$H(Z)=[Y(Z)/X(Z)]=[(b_0+b_1z^{-1}+b_2z^{-2}+b_3z^{-3})\ (1+a1z^{-1}+a2^{-2}+a3z^{-3})$ (3)

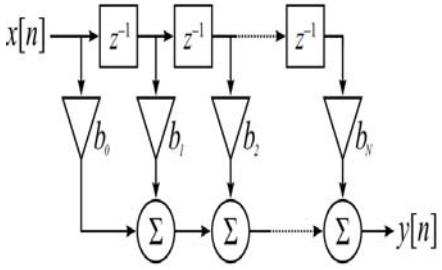

Fig.3.Structure of the FIR filter.

The output is given by the summation of the given input x[n] and the multiplier terms $b_0 b_1 \ldots\ldots b_n$ as given in the following equation.

$$Y[n]=b_0x[n]+b_1x[n-1]+\ldots\ldots..b_kx[n-k]$$

$$Y[n]=\sum b_i x[n-i]. \qquad (4)$$

4.Practical Results:

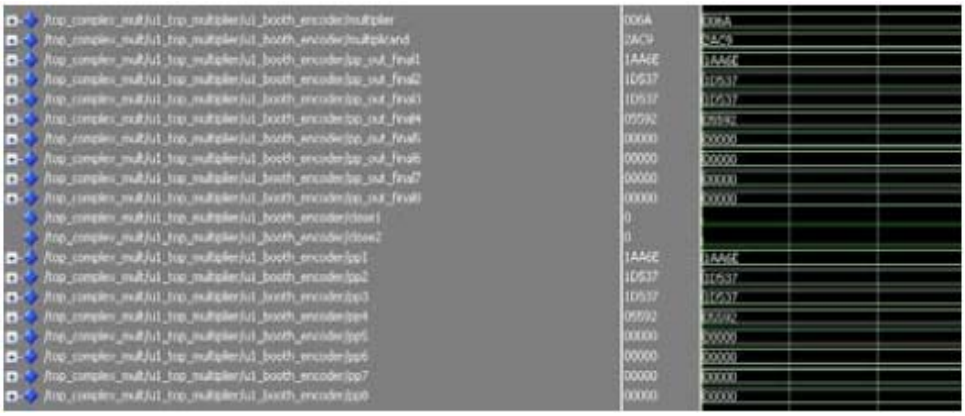

Fig.3.BOOTH ENCODER

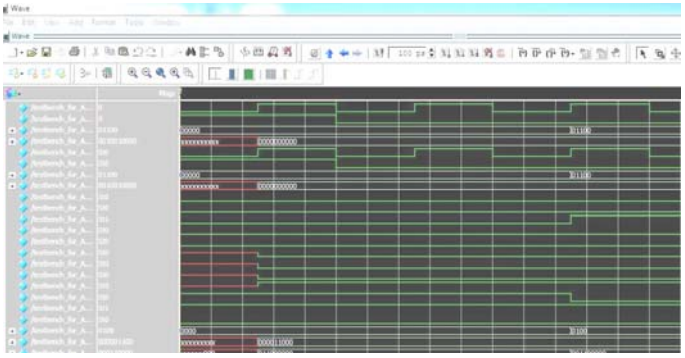

Fig.4.SPST Multiplier with FIR Filter

CONCLUSION :

The SPST technique implemented in booth encoder filter and the FIR filter structure will results in the faster multiplier. The following table shows the comparison of the different multipliers using different logic gates and in case of the FIR filter structure the barrel shifters are used in the circuit. It gives more efficient results than other multiplier structures.

Multiplier Type	Tree Multiplier	Proposed Multiplier Using Registers.	Proposed Multiplier Using AND Gates.	Proposed Multiplier Using Barrel Shifter
Vendor	Xilinx	Xilinx	Xilinx	Xilinx
Device and Family	Spartan 2	Spartan 2	Spartan 2	Spartan 2
Delay	16.235	10.178	6.788	5.2
Power dissipation.	62.91	40	36	32.62
Area(No of Luts used).	444	520	530	142

TABLE.2.COMPARISION OF DIFFERENT MULTIPLIER.

REFERENCES:

[1] "Power Efficient VLSI Architecture for IIR Filter Using Modified Booth Algorithm"by R.Dutta, Surendra Institute of Engineering & Management, West Bengal University of Technology,Siliguri, West Bengal, India.

[2] L.Benini, G.D.Micheli, A.Macii, E.Macii, M. Poncino and R.Scarsi, *"Glitching power minimization by selective gate freezing,"* IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 8, no. 3, pp.287–297, June 2000.

[3] http://www.eecs.tufts.edu/~ryun01/vlsi/verilog_simulation.htm

[4] Hoang Q. Dao, Vojin G. Oklobdzija, *"Application of logical Effect on delay analysis of 64-bit Static Carry- Look ahead Adder"* in 35th Annual Conference on Signals, Systems and Computers, November 4-7, 2001.

[5] http://www.users.encs.concordia.ca/~asim/coen312/Lectures/CLA_adder.pdf

[6] C. S. Wallace, *"A suggestion for fast multipliers,"* IEEE Trans. Electron. Computers, vol. 13, pp. 14-17, Feb.1964.

[7] H. Lee, *"A power-aware scalable pipelined Booth multiplier"* in Proc. of IEEE Int. SOC Conf., 2004, pp. 123–126.

[8] *"Low Power Small Area Modified Booth Multiplier Design for Predetermined Coefficients"* by Yong-eun Kim, Kyung-ju Cho, Jin-gyun Chung, DOI: 10.1093/ietfec/e90, Issue: 3, pp: 694-697.

[9] *"An Area-Efficient Iterative Modified Booth Multiplier Based on Self-timed Clocking"* by Myoung Cheol Shin, Se-Hyeon Kang and In-Cheol Park.

[10] Yong-Eun KIM, Kyung-Ju CHO and Jin-Gyun CHUNG, *"Low power small area modified booth multiplier design for predetermined coefficients"* in IEEE trans. fundamentals, Vol. E90-A, No.3, March 2007.
www.xilinx.com

[11] Denton J. Daily (2004), *"Programming Logic Fundamentals using Xilinx ISE and CPLDs"* in Prentice Hall, 203 pages.

[12] "A spurious power suppression technique for multimedia application" M. Praveen kumar, M.Tech

[13] Prof. K Ashok Babu HOD,SRI INDU COLLEGE OF ENGG&TECHNOLOGYIbrahimpatnam Hyderabad, Andhra Pradesh, India - 501510

[14] "An Efficient Spurious Power Supression Technique (SPST) and its Application on MPEG-4 AVC/H.264Transform and coding design"by kuan-hung chen, kuo-chuan chao, rjinn-shyan wang, yuan-sun chu, jiun-in guo.

[15] "An Efficient Spurious Power Supression Technique (SPST) and its Application on MPEG-4 AVC/H.264Transform and coding design"by kuan-hung chen, kuo-chuan chao,jinn-shyan wang, yuan-sun chu, jiun-in guo