PERFORMANCE EVALUATION OF AN EFFICIENT SINGLE EDGE TRIGGERED D FLIP FLOP BASED SHIFT REGISTERS USING CNTFET

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Abstract

Low power flip-flops are very important for low-power digital designs. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices have shrunk down to nanometer ranges. Due to the usage of millions of components and shrinking process technology, power consumption is drastically high in nano MOSFETs. Hence the paradigm has shifted to Carbon Nano Tube FET. In this paper, impact of 32nM MOSFET and 32nM CNTFET in the design of single edge triggered D-Flip Flop based shift registers are measured in terms of average power, delay, power delay product, rise time and fall time. MOSFET and CNTFET designs are simulated in 1GHz clock frequency and their performances are compared.

***Keywords*: CNTFET, Single Edge Triggered D Flip Flop, power, Power Delay Product, Rise Time, Fall Time.**

1. Introduction

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this era, it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. More switching implies higher average current is expelled and therefore the probability of reliability issues occurring rises. We are moving from laptops to tablets and even smaller computing digital systems. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to be addressed. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's and future integrated chips[10]. Power consumption of Very Large Scale Integrated design is given by generalized relation, $P = CV^2f$ [5]. Since power is proportional to the square of the voltage as per the relation, voltage scaling is the most prominent way to reduce power dissipation. However, voltage scaling is results in threshold voltage scaling which bows to the exponential increase in leakage power. The flip-flops proposed in the literature can be categorized into two ideas. The first idea is to have an additional circuitry for generating internal pulse signals based on clock signal. The second idea is to have two way data path in order to enable sampling of data on either positive or negative clock edges. Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flip-flops [7]. This paper is organized as follows: Section II describes the Ballistic Carbon Nano Tube Field Effect Transistor (CNTFET). Section III describes the CNTFET based single edge triggered D Flip-Flop and Shift Registers. The performance analysis of proposed SET D flip flop based SISO, SIPO, PISO and PIPO shift registers using MOSFET and CNTFET designs are observed and compared in section IV. Paper ends in Section V with the conclusion.

2. Ballistic CNTFET

Three assumptions are essential to assume that a CNTFET is in the ballistic regime: (i) carrier scattering events are quasi-suppressed in the intrinsic channel or carriers in the channel are free from scattering and all carriers propagating towards the drain without scattering back to the source. In this case, the carrier's transport is ballistic and in the ohmic zone, the drain current is expressed with elementary parameters without depending on the carrier mobility. This current depends on the channel length and is proportional to the channel width or

nanotube diameter. (ii) V_{CNT} is defined by four different capacitors: drain (CD), source (CS), quantum (CQ) and gate (CG). Since CG is significantly higher than the three others (particularly when using high-k gate dielectrics), the total capacitance is upper limited by quantum capacitance (iii) CNTFETs operate in quantum capacitance limit. When CG << CQ, the charge at the beginning of the channel is nearly independent of the drain voltage on the contrary [9]. When CG >> CQ, the charge at the beginning of the channel decreases when V_D increases. In the quantum capacitance limit, instead of having the charge constant, the gate holds the nanotube potential constant, equal at the gate potential. The figure 1 shows the structure of ballistic CNTFET device. The limits of scaling the CNTFET will be determined by 2D electrostatics, and scattering and parasitic resistance will likely limit the performance in practice. Model parameters for CNTFET are shown in Table 1.

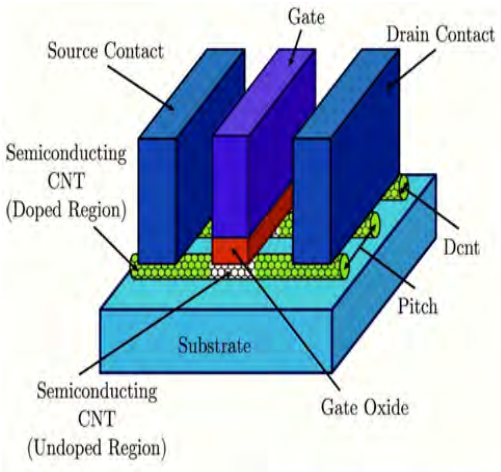


Figure1. A Typical CNTFET Device

Table 1: CNTFET Model Parameters

Parameter	Value
Supply Voltage (V_{DD})	1.0V
Physical channel length (L)	32nm
Diameter of the CNT (d)	1.487nm
The length of doped CNT source-side extension region. (L_{SS})	32nm
The length of doped CNT drain-side extension region.(L_{DD})	32nm
The thickness of high-k top gate dielectric material (T_{OX})	4nm
The dielectric constant of high-k top gate dielectric material (K_{OX})	16
The distance between the centers of two adjacent CNTs within the same device.	20nm
Chiral Vector	(19,0)

3. CNTFET based SET D-Flip Flop and Shift Registers

Proposed SET D-flip flop is designed from power pc603 SET D-FF [1]. The CNTFET based flip flop design is shown in figure 2. This flip-flop is a Master Slave flip flop structure and it consists of two data paths. As conventional n-type pass transistors give weak high output, in the proposed design the n-type pass transistors are followed by an inverter to give strong high output. Hence the proposed SET D-Flip Flop is free from threshold voltage loss. Thus the designed Single Edge Triggered D-Flip-Flop has become more efficient in terms of area, power and speed and hence provides better performance than conventional Flip Flops. Impact of the proposed D FF is analyzed in four types of shift registers.

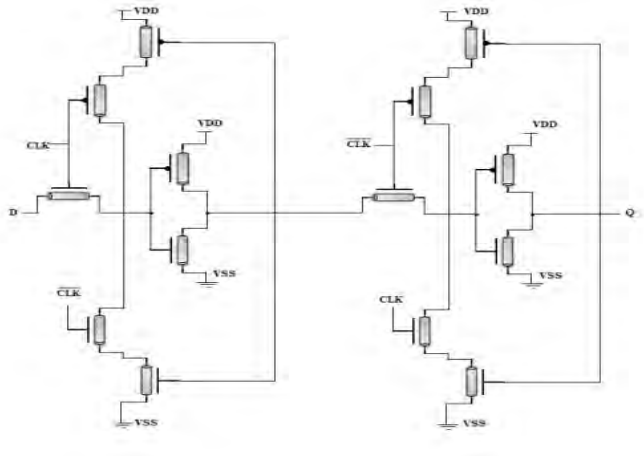


Figure2. Proposed SET D Flip Flop Using CNTFET

The shift registers are Serial in Serial out shift register(SISO), Serial in Parallel out shift register(SIPO), Parallel in Parallel out shift register(PIPO) and Parallel in Serial out shift register(PISO). Storage capacity of a register is the total number of digital data bits it can retain. Each stage in a shift register represents one bit of storage

capacity. The four bit shift registers are designed using proposed SET D-flip flop in CNTFET technology. Serial in serial out shift register accept data input serially on a single line and it gives the stored information on its output also in serial form. CNTFET based serial in and serial out shift register design is shown in figure 3. Serial in parallel out shift register also accept data input in serial form. Once the input data is given, it may be either read off at each output simultaneously, or it can be shifted out and replaced. This configuration allows conversion from serial to parallel format. CNTFET based Serial in parallel out shift register design is shown in figure 4.

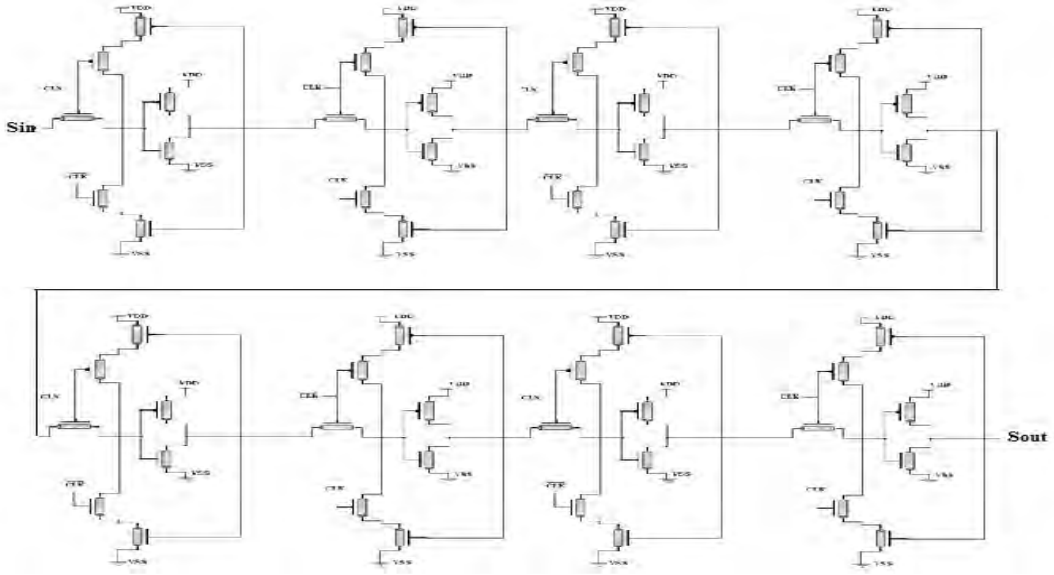


Figure3. CNTFET based Serial in-Serial out Shift Register

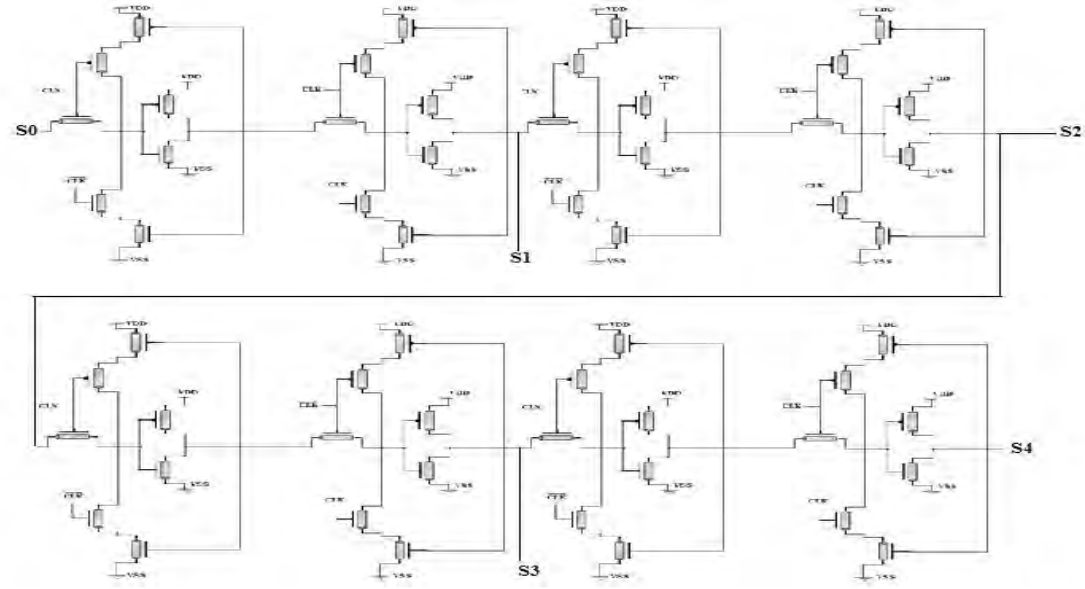


Figure4. CNTFET based Serial in-Parallel out Shift Register

Parallel in Serial out Shift Register configuration has the data input on lines d1 through d4 in parallel form. To write the data to the register, the write/shift control line should be held low. To shift the data, the write/shift control line is brought high and the registers are clocked. Figure 5 arrangement shows CNTFET based design of PISO shift register. For parallel in parallel out shift register, all data bits occur as parallel outputs immediately following the simultaneous entry of the data bits with respect to clock. The circuit design of parallel in parallel out shift register constructed by CNTFET based proposed SET D flip-flops and shown in figure 6.

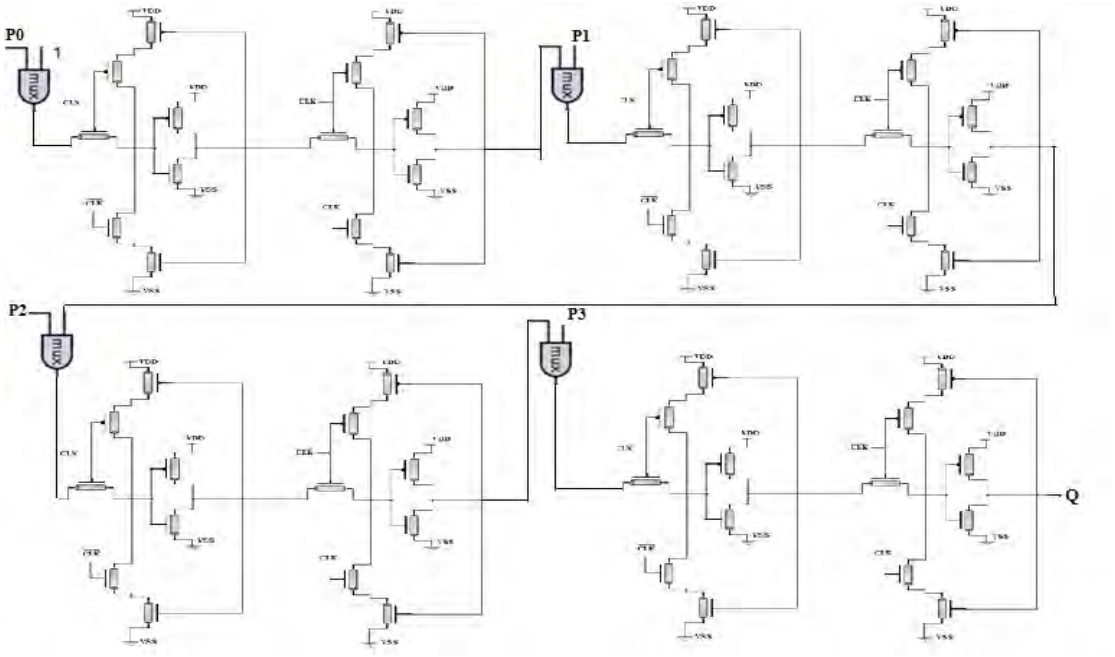


Figure5. CNTFET based Parallel in Serial out Shift Register

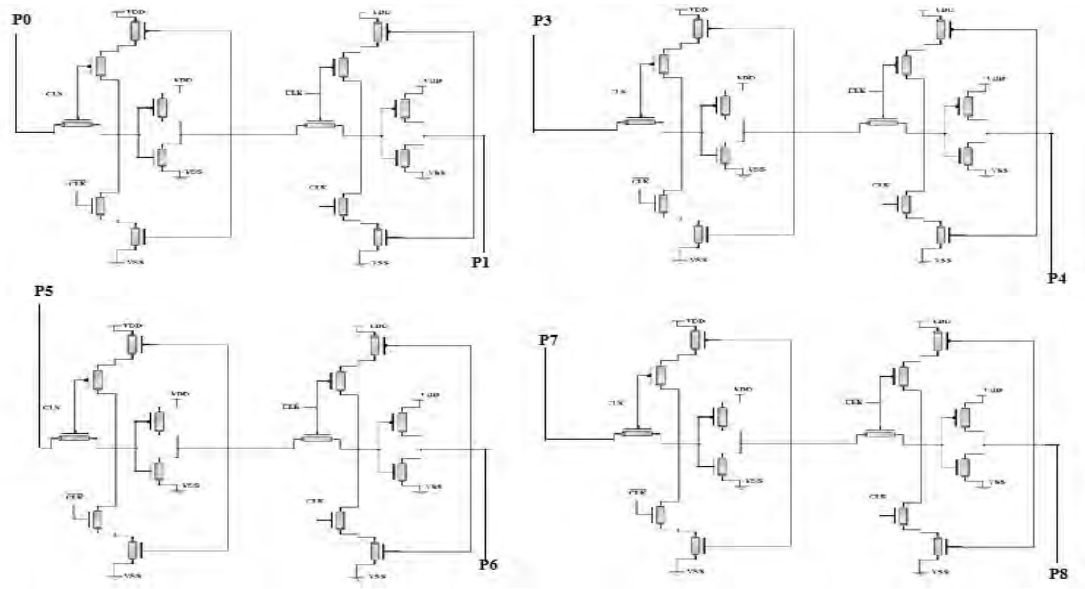


Figure6. CNTFET based Parallel in Parallel out Shift Register

4. Performance Analysis

To evaluate the performance of proposed SET D-FF based shift registers are designed using MOSFET and CNTFET in 32nm technology. Simulations are carried out using HSPICE tool in nominal conditions with operating frequency at 1GHz. Transient analysis of the proposed SET D-Flip flop using CNTFET is shown in figure 7 and the transient analysis of SET D-Flip flop based shift registers using CNTFET are shown in figures 8, 9, 10 and 11.

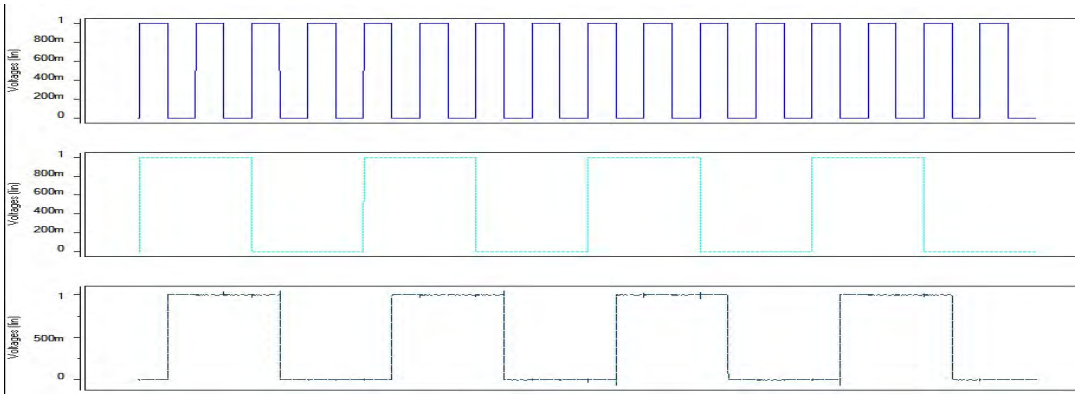


Figure7. Transient analysis of a proposed SET D-FF using CNTFET

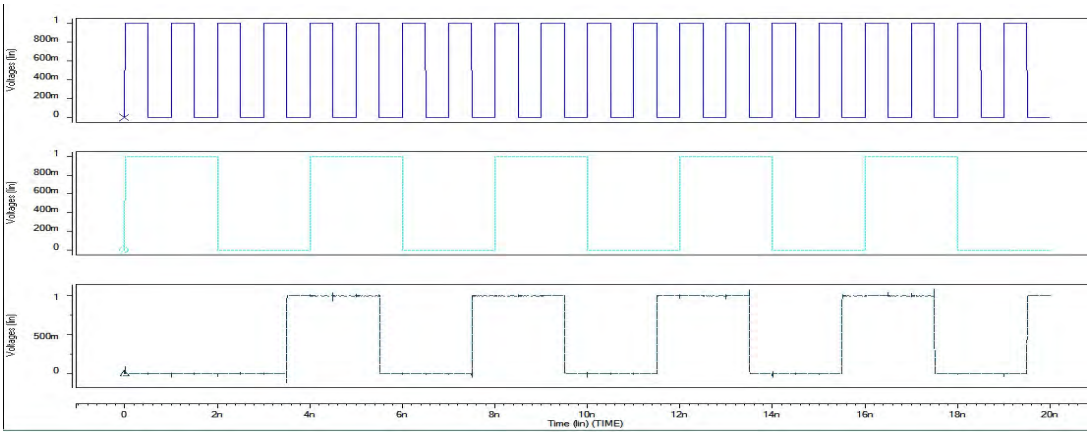


Figure8.Transient analysis of a proposed SET D-FF based SISO Shift Register using CNTFET

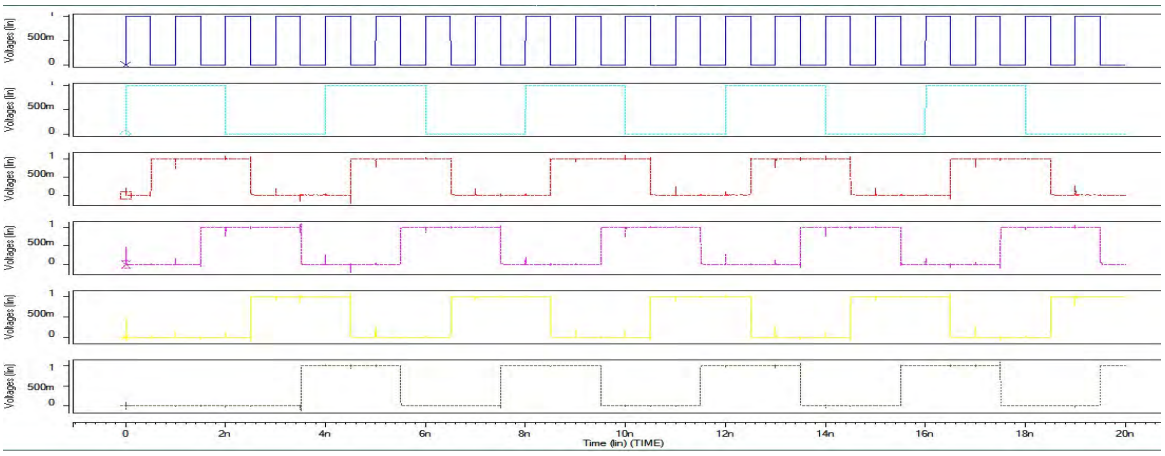


Figure9.Transient analysis of a proposed SET D-FF based SIPO Shift Register using CNTFET

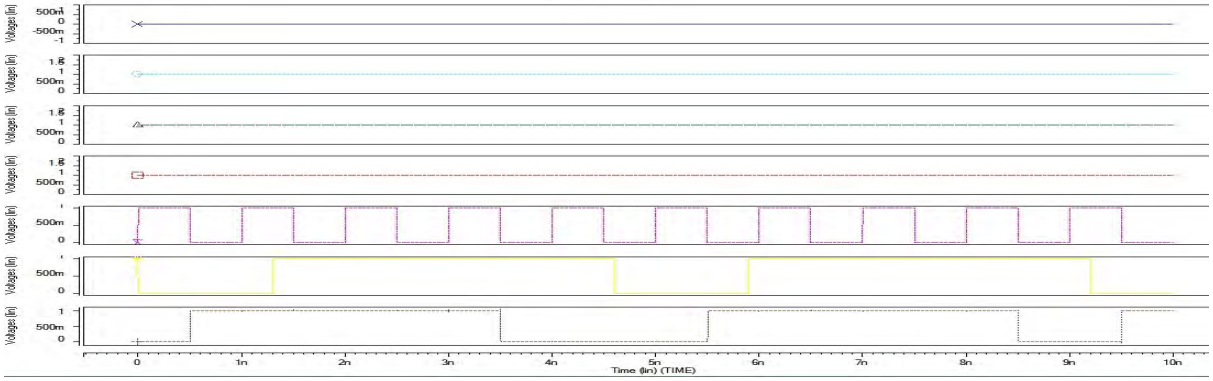


Figure10.Transient analysis of a proposed SET D-FF based PISO Shift Register using CNTFET

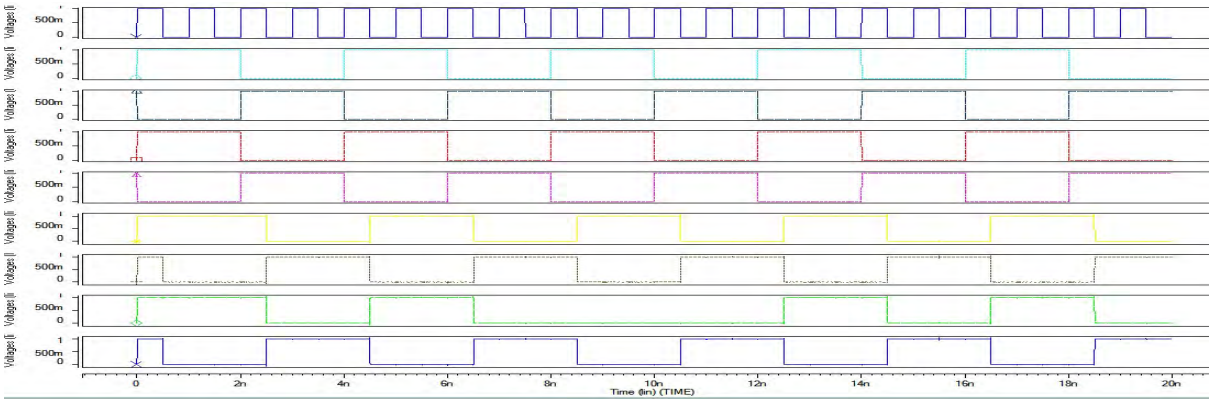


Figure11.Transient analysis of a proposed SET D-FF based PIPO Shift Register Using CNTFET

The performance of the CNTFET based SET D-Flip Flop and shift registers are evaluated by comparing the average power, delay, power delay product (PDP), rise time and fall time with CMOS design in 32nm technology. A PDP based comparison is appropriate for low power portable systems in which the battery life is the primary index of energy efficiency. The tables 2 and 3 furnished the performance of the designs with the operating voltage of 1V and the operating frequency at 1GHz.The performances are compared in figures 12, 13, 14, 15 and 16.

Table 2: Performance Analysis of MOSFET and CNTFET Designs

	AVG POWER(W)		**DELAY(s)**		**PDP(J)**	
DESIGN	MOSFET Design	CNTFET Design	MOSFET Design	CNTFET Design	MOSFET Design	CNTFET Design
D-FF	2.184e-06	0.779e-07	16.361p	3.1010p	35.73e-18	2.415e-19
SISO	2.372e-05	0.036e-05	3.016n	3.0038n	7.15e-14	0.108e-14
SIPO	2.372e-05	0.036e-05	18.32p 1.018n 2.017n 3.016n	4.7310p 1.0039n 2.0042n 3.0038n	43.45e-17 2.14e-14 4.78e-14 7.15e-14	0.170e-17 0.036e-14 0.072e-14 0.108e-14
PIPO	8.73e-06	0.314e-06	16.367p	4.223p	142.88e-18	1.32e-18
PISO	10.32e-06	0.791e-06	3.026n	3.0058n	31.22e-15	2.37e-15

Table 3: Rise Time and Fall Time Analysis of MOSFET and CNTFET Designs

	RISE TIME(s)		**FALL TIME(s)**	
DESIGN	MOSFET Design	CNTFET Design	MOSFET Design	CNTFET Design
D-FF	4.677p	2.0683p	7.445p	2.538p
SISO	4.246p	2.807p	5.890p	2.727p
SIPO	4.679p 5.546p 4.890p 4.246p	2.284p 2.87p 2.54p 2.807p	5.780p 6.430p 5.769p 5.890p	3.24p 3.004p 3.246p 2.727p
PISO	8.769p	2.997p	13.799p	3.76p
PIPO	6.823p	3.618p	4.792p	2.472p

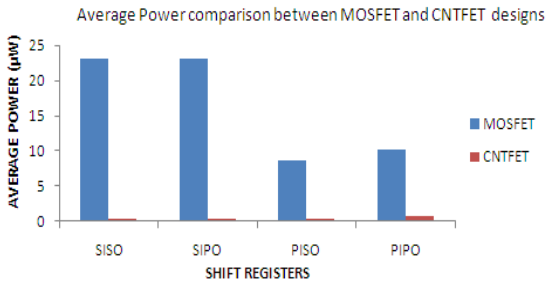


Figure12. Average Power analysis of MOSFET and CNTFET Designs

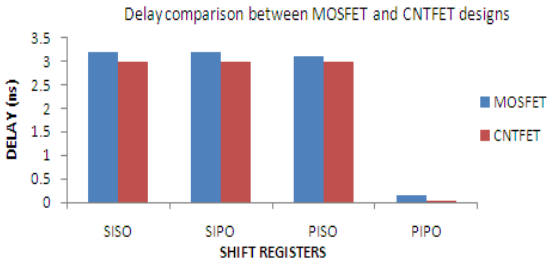


Figure13. Delay analysis of MOSFET and CNTFET Designs

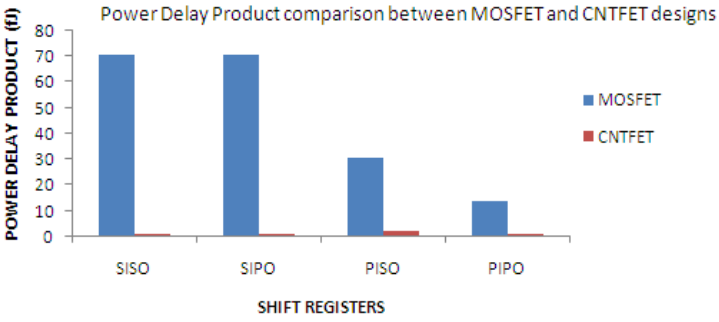
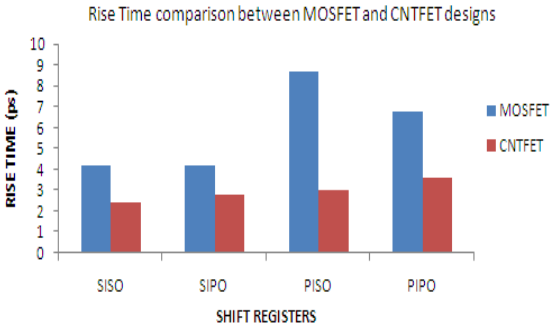


Figure14. Power Delay Product analysis of MOSFET and CNTFET Design



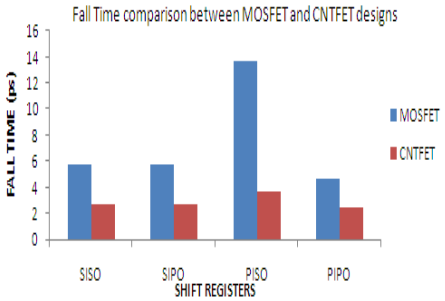


Figure15. Rise Time analysis of MOSFET and CNTFET Design
Figure16. Fall Time analysis of MOSFET and CNTFET Design

5. Conclusion

In this paper, we have designed an efficient single edge triggered D-FF based shift registers in 32nm CMOS and CNTFET technologies. Flip Flop and Shift registers are simulated in HSPICE with operating voltage of 1V and operating frequency at 1GHz in MOSFET and CNTFET designs and compared the performances. CNTFET based shift registers have 65% less power consumption, delay has also decreased and power delay product (PDP) has been reduced 66% than MOSFET design. The rise time and fall time has also been decreased. The CNTFET based flip flop and shift registers are more efficient in average power, delay, power delay product, rise time and fall time. Hence from performance analysis of an efficient single edge triggered D-FF based shift registers using CNTFET is more efficient for low power and high performance applications.

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