

Design of JK Flip-Flop using MODFET Technology

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Abstract

The pertinent choice of flip-flop topologies is an essential importance in the design of VLSI integrated circuits for high speed and high performance MODFET circuits. Understanding the suitability of flip-flops and selecting the best topology for a given application is an important issue to fulfill the need of the design to satisfy low power and high performance circuit. This paper enumerates high speed design of JK- flip-flop using AlGaAs/GaAs MODFET. The proposed Flip Flop is having less number of transistors than existing designs. Simulation results show lowest average power and least delay than existing designs. This Flip-Flop having less number of transistors. It can be efficiently used in VLSI ICs. In the verification by simulation, the proposed flip-flops appear to have better speed of operation. It is simple and suitable to SPICE simulation of hybrid digital ICs.

Keywords: Flip-Flop, MODFET, delay, PDP, power consumption.

INTRODUCTION

A flip-flop is a bi-stable circuit which stores a logic state of 0 or 1 in response to a clock pulse with one or more data inputs. In digital circuit design, large proportion contributes to synchronous design and they are operated based on the clock signal to reduce the complexity of the circuit design. Technology scaling of a transistor feature size has provided a remarkable innovation in silicon industry for the past few decades. Designers are striving for semiconductor area, higher speed, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. With the increasing use of mobile devices, consumer electronics markets demand a stringent constraint on reducing the power dissipation. In order to reduce the complexity of circuit design, the digital circuits are designed to be synchronous circuits. The memory elements in a sequential circuit are called flip-flops. The JK flip flop is an essential building block of digital logic. It is a device that can store a single piece of information known as a bit. The JK flip flop was chosen for this project because it is a more versatile flip flop when compared to the D- and T-types. Both the D- and T-type flip flops can be simulated by the JK flip flop by simple manipulation of the inputs J and K. For example, if one tied together the J and K inputs, a T flip flop will result. The flip flop in this design has several inputs: J, K, Set (S), Reset (R), Enable (E), and a Clock (CLK). The J and K inputs are used to manipulate the outputs Q and \sim Q. The Set and Reset inputs are used to declare a particular output of set or reset regardless of the states of J and K. The Enable input is used to make the flip flop respond to its inputs. When Enable is logic 1, the flip flop behaves normally to its inputs, when it is logic 0, it will not respond. Logic 1 represents VDD = 5 V while logic 0 represents 0 V. The flip flop used in this design is a master-slave configuration. Each flip flop has complementary clock signal making one active while the other is not. The state of the flip flop, Q, is update on the falling edge of the clock signal. The basic components that comprise this flip flop are nand gates, and not gates. The Modulation doping field effect transistor has demonstrated characteristics which make it highly suitable for high performance high speed system. In this paper describes high speed JK-flip flops using MODFET technology. In this paper, we designed logic gates using RTL logic, so the number of transistors used for making Flip Flops is very less and the area of the Flip Flops is also reduced. The design for low power issues can't be overcome without precised power prediction and optimization tools. Therefore, the critical need for certain tools to calculate power dissipation during the design to meet the power constraints to ignore the costly redesign effort.

1.CIRCUIT DESIGN

1.1. JK FLIP-FLOP

The JK flip flop (JK means Jack Kilby, engineer of Texas instrument, who invented it) is the most versatile flip-flop and the most commonly used flip flop. Like RS flip-flop, it has two data inputs, J and K, and an EN/clock pulse input, Note that in the following circuit diagram NAND gates are used instead of NOR gates. It has no undefined states, however. The basic fundamental difference of this device is feedback paths to the AND gates of the input, i.e. Q AND with K and Q' with J and CP. The JK flip-flop has the following characteristics: If any one input (J or K) is logic 0, and the other is logic 1, then the output is set or reset (by J and K respectively), just like the RS flip-flop. If both inputs are 0, then its remains in the same state as it was before the clock pulse occurred; again like the RS flip flop. CP has no effect on the output. If both inputs are high, however the flip-flop changes state whenever a clock pulse occurs; i.e., the clock pulse toggle the flip-flop again and again until the CP goes back to 0 as shown in the shaded rows of the characteristic table below. The logic diagram of JK flip flop is shown in the fig.1 and circuit diagram shown in the fig.2.

Table 1. Characteristic Table of JK Flip Flop

Q _n	J	K	Q _{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1(Toggle, \bar{Q}_n)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0(Toggle, \bar{Q}_n)

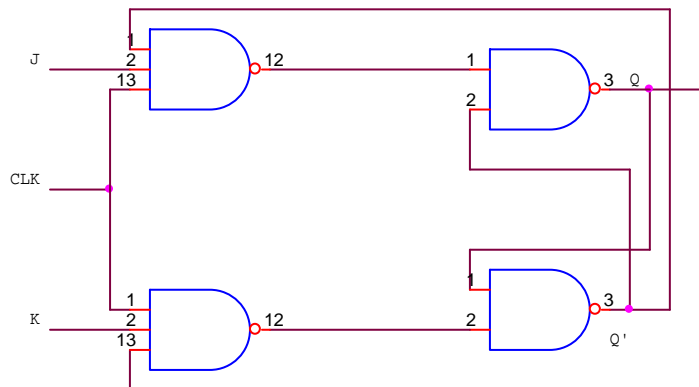


Fig. 1. Logic diagram of JK Flip Flops using NAND gate

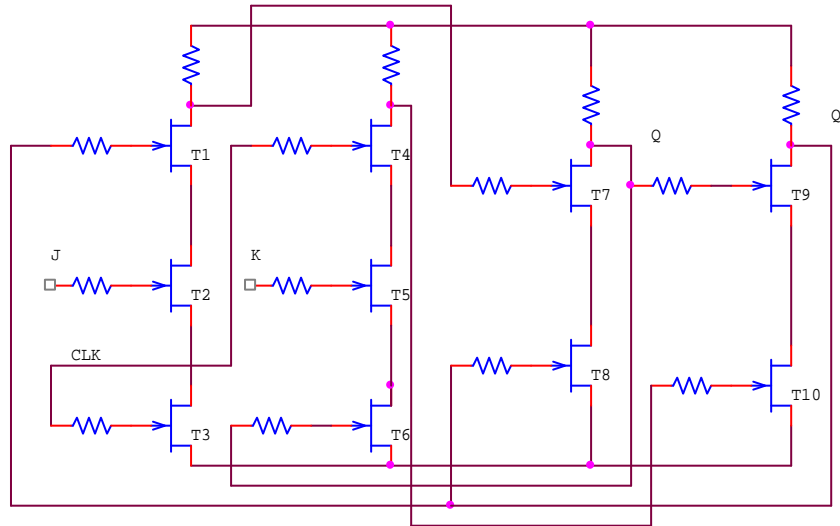


Fig. 2. Circuit diagram of JK Flip Flops using NAND gate

1.2. MASTER-SLAVE JK FLIP-FLOP

Although JK flip-flop is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race" if the output Q changes state before the timing pulse of the clock input has time to go "OFF", so the timing pulse period (T) must be kept as short as possible (high frequency). This is not possible with modern TTL IC's the much improved Master-Slave J-K Flip-Flop was developed. This will eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse. The master-slave JK flip flop consists of two flip flops arranged so that when the clock pulse enable the first, or master, it will disables the second, or slave. When the clock changes state again (i.e., on its falling edge) the output of the master latch is transferred to the slave latch. The logic diagram of Master slave JK flip flop is shown in the fig.3 and circuit diagram shown in the fig.4.

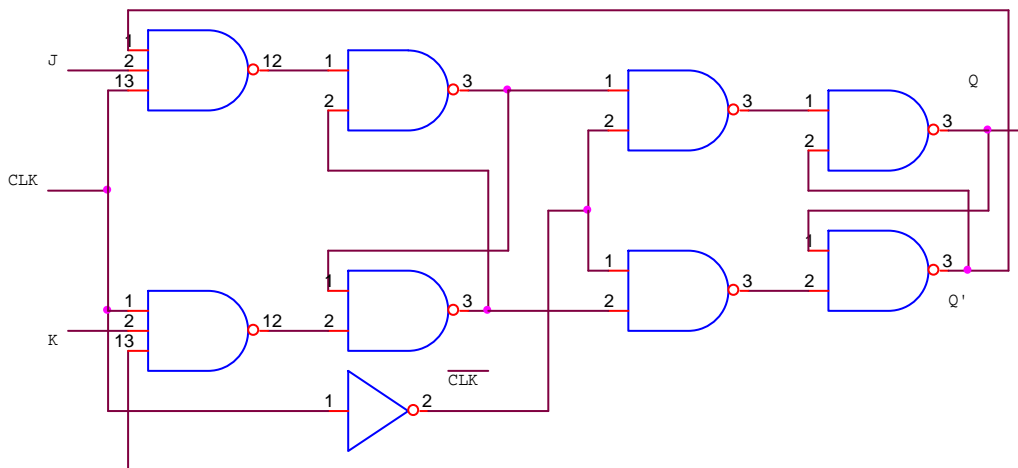


Fig. 3. Logic diagram of JK Flip Flops using NAND gate

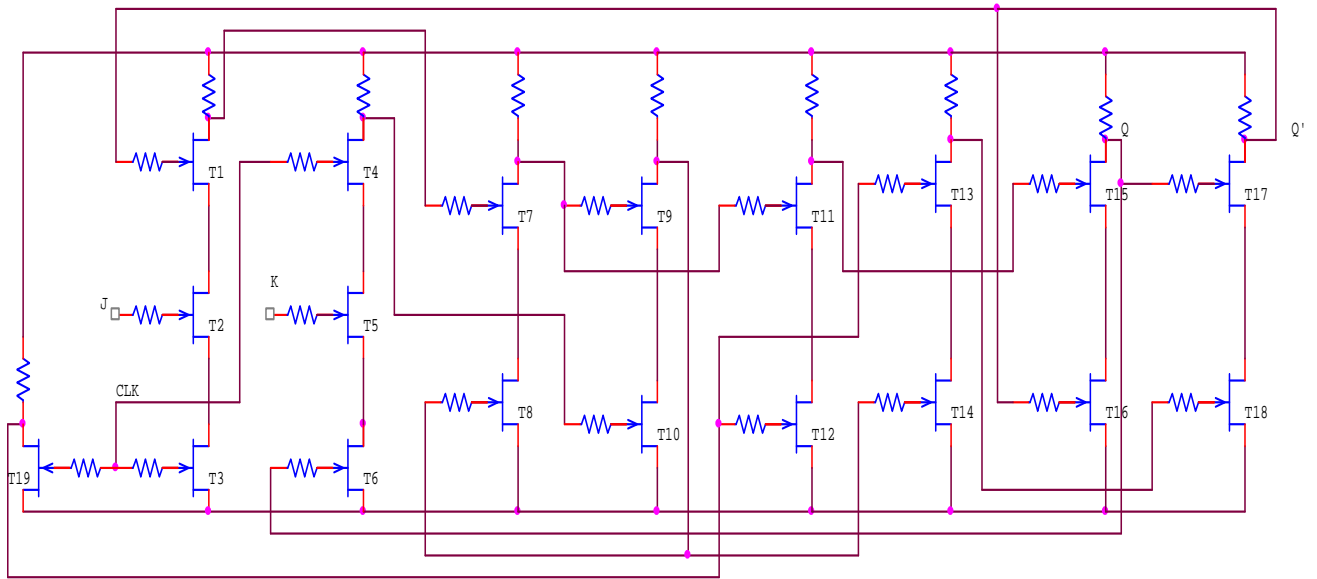


Fig. 4. Circuit diagram of JK Flip Flops using NAND gate

2. Performance Analysis

The logic operations of the circuits were first examined by simulation using P-Spice simulation software. The simulated input-output waveform is depicted in Figures. The logic operation is found to be correct. For J-K flip-flop the simulation waveform is shown in the Figure 5. For Master slave J-K flip-flop the simulation result is shown in Fig.6. The results obtained from the simulation are found to be satisfactory. The logic operations of the circuits are found to be satisfactory.

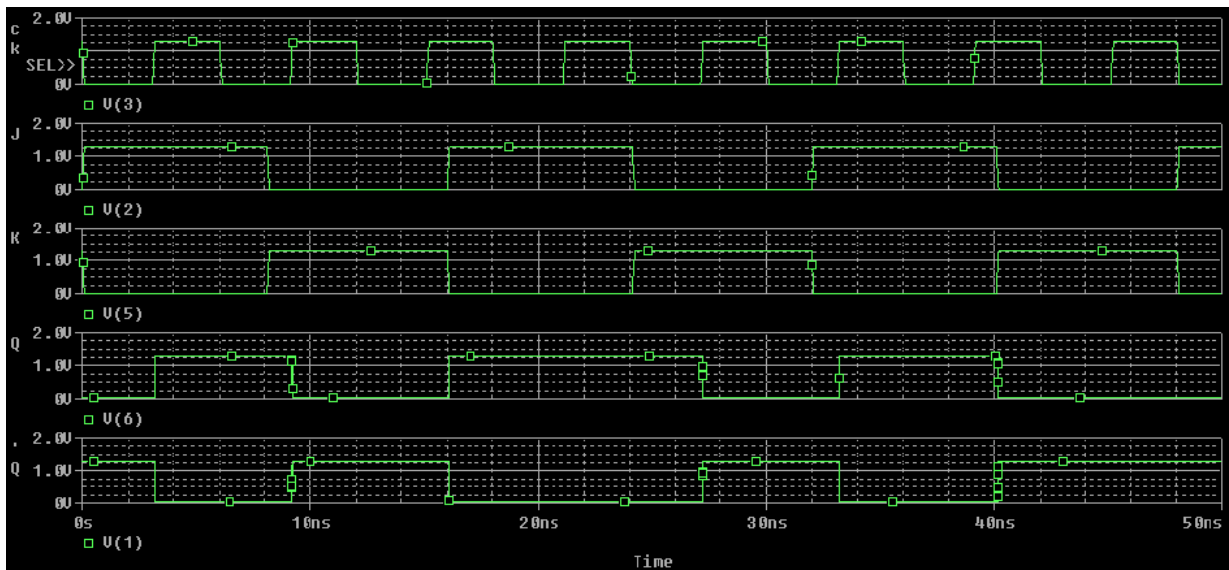


Fig. 5. Output waveform for proposed JK Flip Flops

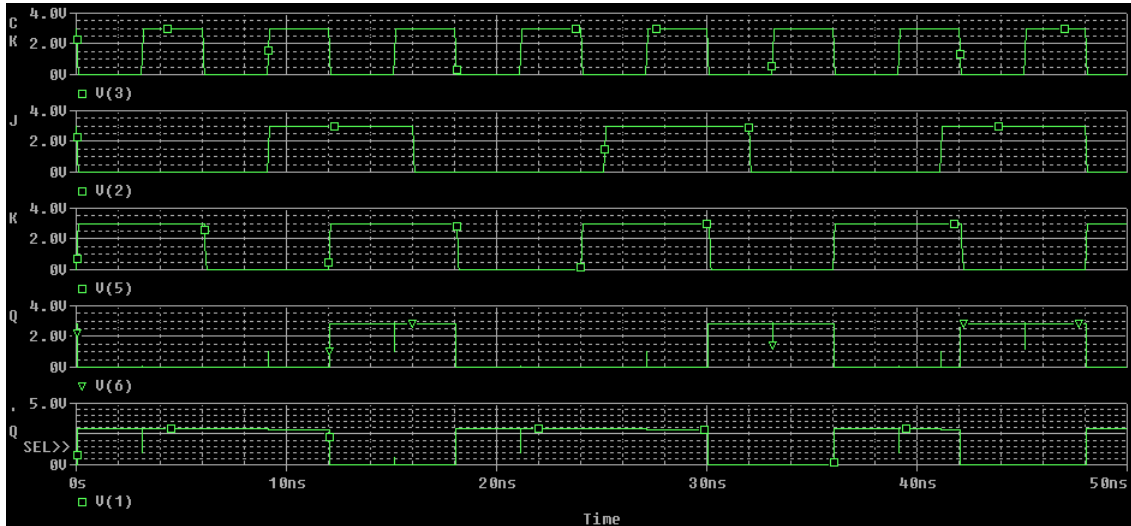


Fig. 6. Output waveform for proposed Master Slave JK Flip Flops

3. Comparison of MOSFET, and MODFET JK flip-flops

The proposed JK and Master Slave JK flip flop using MODFET is designed and compared with several existing Flip-Flops. Each Flip-Flop is optimized for power delay product. The proposed flip flop is having lesser number of clocked transistors than the other flip flop. Simulation results for power, delay, PDP (power delay product) and area at nominal conditions for the Flip-Flops are summarized in Table 3. And comparison graph is shown in the fig.7a,7b,7c.

Table 2. Comparison of MOSFET, and Proposed MODFET D flip flops

Device	Delay (*10 ⁻¹² Sec)	Power (*10 ⁻⁶ W)	PDP (*10 ⁻¹⁷ J)
Con. DFF	76	3.1	23.56
Proposed DFF	15	2.9	4.35

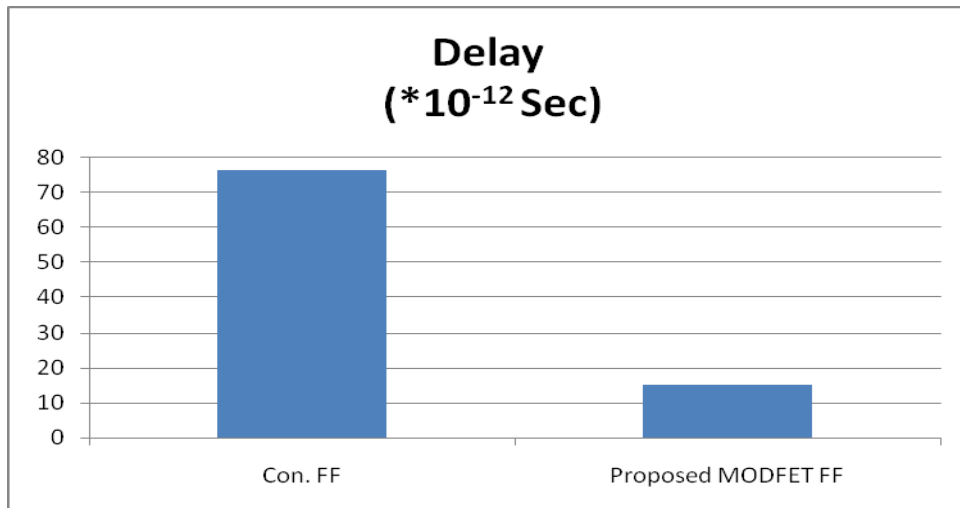


Fig. 7a. Comparison of MOSFET, and MODFET – Delay

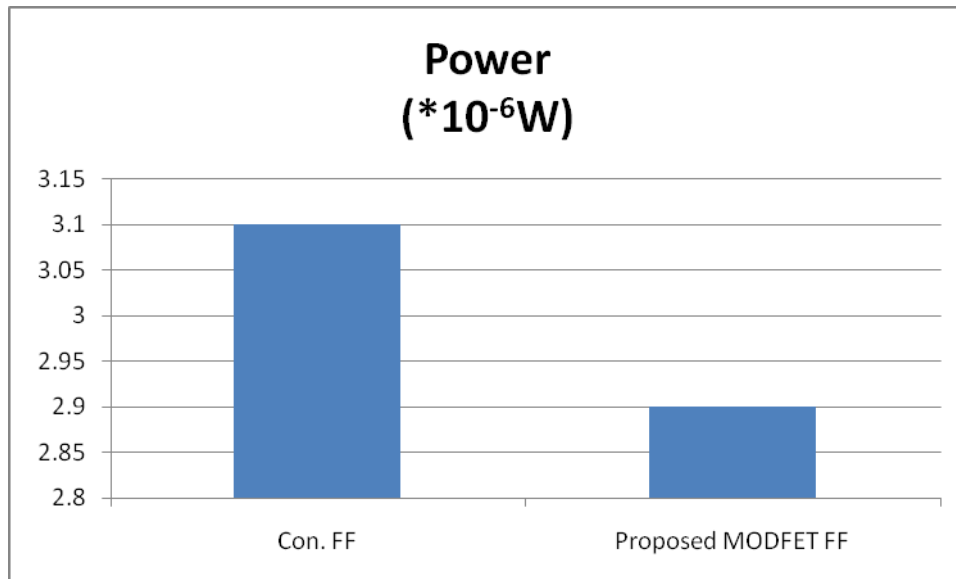


Fig. 7b. Comparison of MOSFET, and MODFET - Power

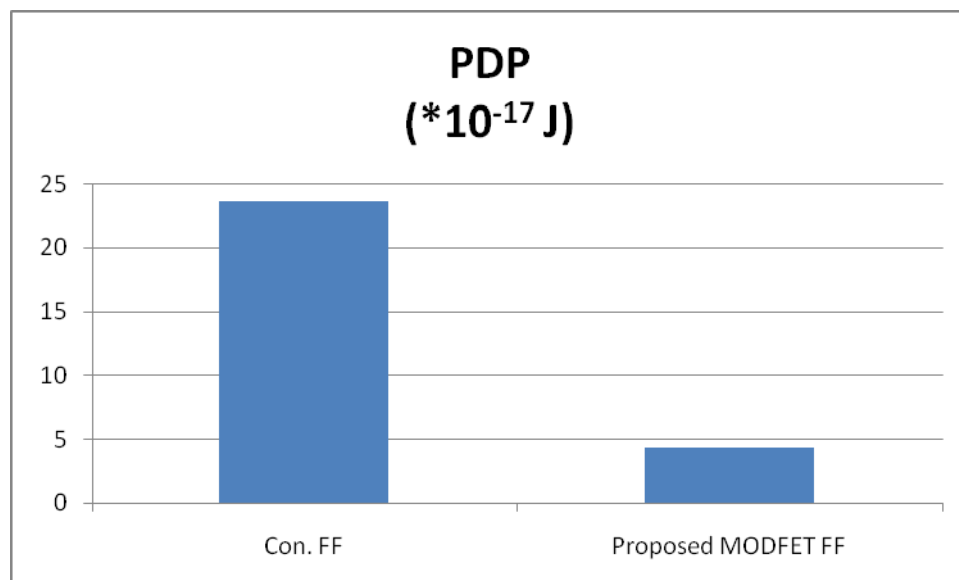


Fig. 7c. Comparison of MOSFET, and MODFET – PDP

4. Conclusion

In this paper, we have designed an efficient JK and Master slave JK flip flop using AlGaAs/GaAs MODFET technologies. The Flip Flop are simulated in PSPICE with operating voltage of 1V. MODFET based flip flop have 20% less power consumption, delay also decreased and power delay product (PDP) has been reduced 80% than flip flop using MOSFET design. The rise time and fall time also decreased. The MODFET based flip flop are more efficient in average power (p), delay (d), power delay product (pdp), rise time and fall time. Hence from performance analysis of JK and Master slave JK flip flop using MODFET is more efficient for low power and high performance applications.

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