Comparison between simulations of different RBSD Adder Circuits

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Abstract*:*Adders are the key element of the arithmetic unit, especially fast parallel adder. Redundant Binary Signed Digit (RBSD) adders are designed to perform high-speed arithmetic operations. The RBSD Number System is gaining popularity due to the properties of carry-free addition / subtraction. In computational environment it is not convenient for manual computations but useful in designing high-speed arithmetic machines. This number system eliminates the carry / borrow propagation chains which reduces the computational time and enhances the speed of the machine. In this paper the circuit of fast RBSD adder cell proposed by Kal and Rajashekhar in 1990 and modified by N.Sharma in 2006, are designed using Hardware Discriptive Language and simulated on modelsim simulator.

Keywords: RBSD adder, carry free addition,VHDL, high speed arithmetic.

1.Introduction

The speed of arithmetic processor depends upon the speed and the arrangements of the representation results in different arithmetic hardware design. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. With a binary number system, the computation speed is limited by the formation and propagation of carry especially as the number of bits increases. In order to reduce or restrict the delay caused by carry propagation in the arithmetic operations, the operands can be represented in some special number systems other than binary .Signed –digit representation limit carry propagation to one position to the left during the operations of addition and subtraction in digital computers. Carry-propagation chains are eliminated by use of redundant representation for operands. In this method, each digit of a positional constant radix number representation with an integer radix r is allowed to assume q values [1]

r+2 <=q<=2r-1

Both positive and negative digit values are allowed. The purpose of signed digit representation is to allow addition and substraction of two numbers in which no serial signal propagation is required along the adder; i.e., the time duration of the operation is independent of the length of the operands and is equal to the time required for addition or substraction of two digits.

2.Redundant Binary Signed Digit Number System:

The RBSD number system is a numeral system that uses more bits than needed to represent a single binary digit so that most numbers have several representations. The credit of this number system goes to Avizienis 1961 [1]. According to him the RBSD numbers can be represented using the digit set {1, 0, -1} unlike binary number system, which is represented, with digit set {0,1}. The decimal value of RBSD number can be calculated by following relation.

$$\sum_{i=0}^{n-1} xi\ 2^{i} \qquad \text{……..(2.1`)}$$

Example 1:

Conversion of binary number to RBSD number system

$X=(24)_{10}=(11000)_2$

For augends we will take -1 for 1 & 0 for 0,and addend wil remain the same.

$\bar{1}\ \bar{1}\ 0\ 0\ 0$
$1\ 1\ 0\ 0\ 0$
$1\ 0\text{-}1\ 0\ 0\ 0$ $(24)_{10}$ in RBSD

Conversion of RBSD number system to binary

$(010\bar{1}000)rbsd= 0*2^6+1*2^5+0*2^4+0*2^3+0*2^2+0*2^1+0*2^0 =(24)10$

3.Rbsd Addition Technique:

The RBSD addition technique is known as "two transfer addition technique". Two transfer addition is computed in three successive stages and described by following equations[9]:

$$\text{(i)}\quad x_i+y_i=w_i+2t_{i+1} \qquad \ldots\ldots(3.1)$$
$$\text{(ii)}\quad w_i+t_i=w'_i+2t'_{i+1} \qquad \ldots\ldots(3.2)$$
$$\text{(iii)}\quad S_i=w'_i+t'_i \qquad \ldots\ldots(3.3)$$

Where x_i, y_i are operand digits, w_i (w'_i), t_i (t'_i) are the intermediate sums and transfer digits respectively and S_i is the final RBSD sum. The sum of the operand is realized into three steps as:

- In first step the transfer digit is $|t_{i+1}| = 1$ only if $|x_i + y_i| \geq 1$
- In second step the transfer digit $|t'_{i+1}| = 1$ only if $|w_i + t_i| = 2$ under these conditions w'_i and t'_i cannot be both 1 or $\bar{1}$ and
- In third step the sum digits is obtained by carry fee addition of w'_i and t'_i.

Example 2: Addition of both negative numbers

Addition of (-43) and (-150) in RBSD

(+43) = 0 0 1 0 1 0 1 1 (Binary)

(-43) = 1 1 0 1 0 1 0 1 (2's Complement)

(-43) = 10-11-11-11-1 (RBSD Representation)

(+150) = 1 0 0 1 0 1 1 0 (Binary)

(-150) = 0 1 1 0 1 0 1 0 (2's Complement)

(-150) = 010-1 1-1 1-10 (RBSD Representation)

si* =(-1 0 1 0 0 0 0-1 1) = (-256+64-2+1) = (-193)

Addition of one negative and one positive number

Addition of (-12) and (18) in RBSD

x = 18			1	-1	0	1	-1	0
y = -12			0	-1	1	-1	0	0
W			-1	0	-1	0	1	0
t		1	-1	1	0	-1	0	
w´		1	0	1	-1	-1	1	0
t´	0	-1	0	0	0	0	0	
S	0	0	0	1	-1	-1	1	0

4.Logic Design Of Rbsd Adder Circuit:

Using equation 1-5, Kal and Rajashekhar, 1990 designed a RBSD Adder cell as shown in figure 1 . This cell was made by AND, NOR, XOR, OR, and NOT gates which is used for the addition of two 2- bit RBSD numbers.[8]

$$d_i=m_i \text{ xor } \overline{x_i^+}\,\overline{x_i^-} \text{ xor } \overline{y_i^+}\,\overline{y_i^-} \qquad \ldots\ldots\ldots\ldots\ldots\ldots(4.1)$$

$$m_{i+1}=x_i^+ y_i^+ \qquad \ldots\ldots\ldots\ldots\ldots\ldots(4.2)$$

$$b_{i+1}=\overline{m_i}\,\overline{x_i^+}\,\overline{x_i^-} + x_i^+ y_i^+ + \overline{y_i^+}\,\overline{y_i^-}\;\overline{m_i} + \overline{x_i^+}\,\overline{x_i^-}\;\overline{y_i^+}\,\overline{y_i^-} \qquad .(4.3)$$

$$s_i^+=\overline{d_i}\,b_i \qquad \ldots\ldots\ldots(4.4)$$

$$s_i^-= d_i \overline{b_i} \qquad \ldots\ldots\ldots\ldots(4.5)$$

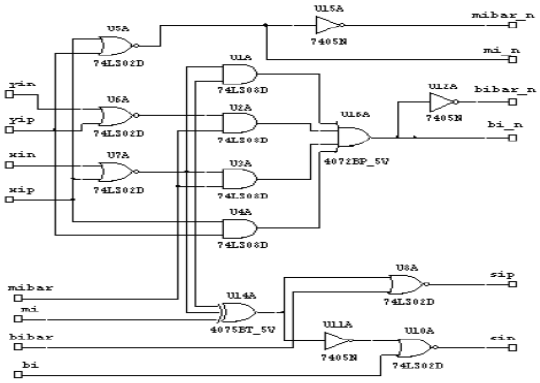


Figure.1. Logic circuit of Basic RBSD adder cell

The adder cell designed by Kal and Rajshekhar, 1990 has been redesigned by the N Sharma in 2006 using universal logic gate i.e. NOR gates only which is shown in figure 2.

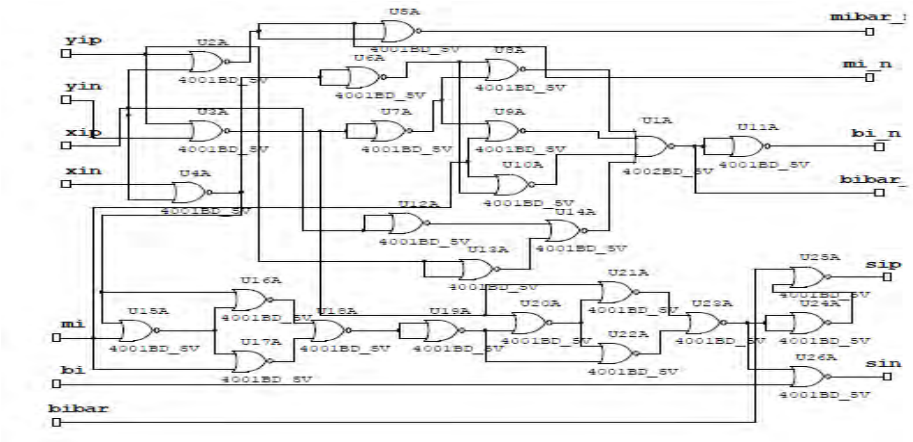


Figure 2. Logic circuit of Adder Cell using NOR-NOR

5.Simulation Results:

Logic design of basic RBSD adder cell is designed using Hardware Discriptive Language .This code is then simulated with the help of Modelsim .

The simulation result of Basic RBSD adder is shown in figure 3,4 & 5.

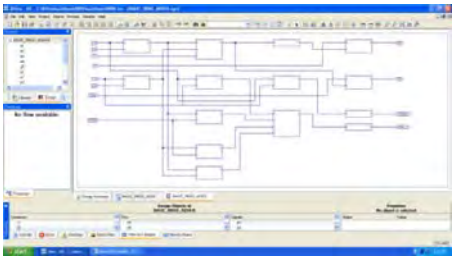


Figure.3 Block Diagram of Basic RBSD Adder Cell

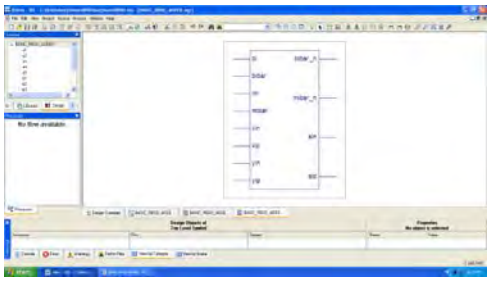


Figure.4 Internal Architecture of Basic RBSD Adder Cell

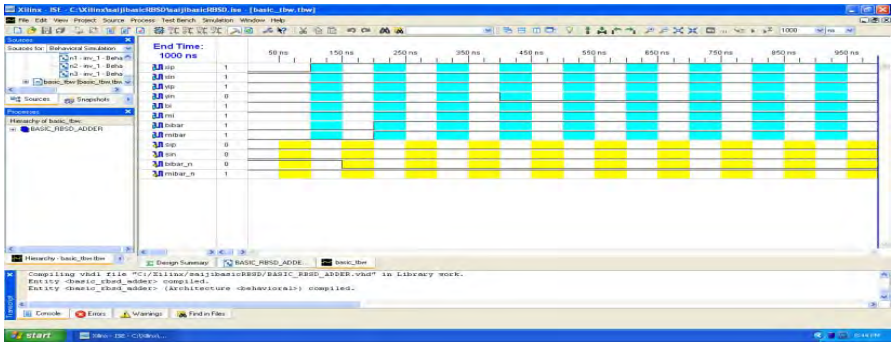
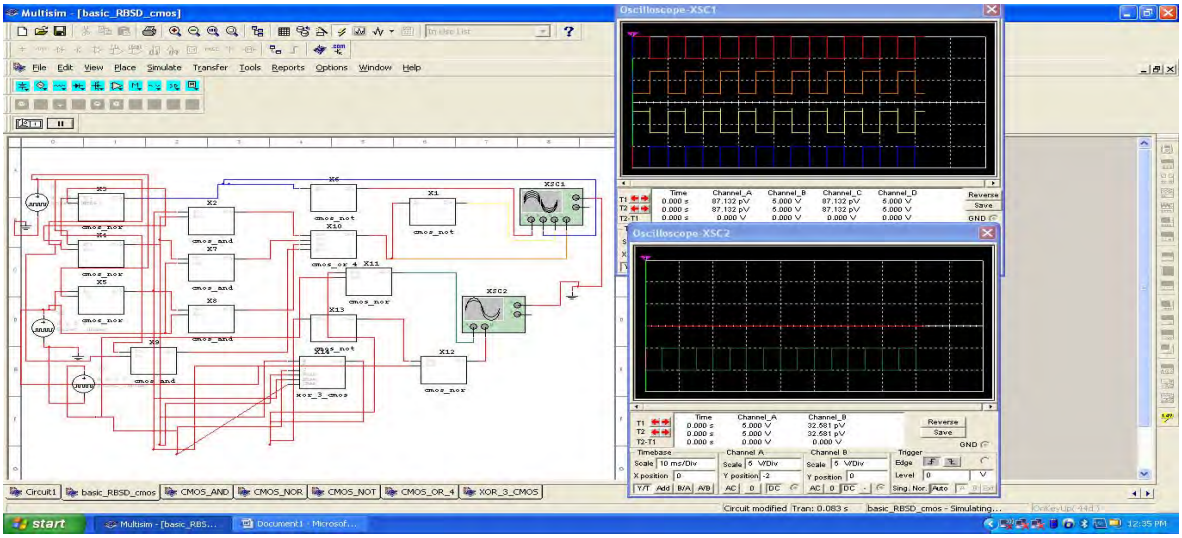


Figure.5 Simulation Result of Basic RBSD Adder Cell

FET Implementation of Basic RBSD Adder Cell



The simulation result of RBSD adder (NOR-NOR) is shown in figure 6,7 & 8.

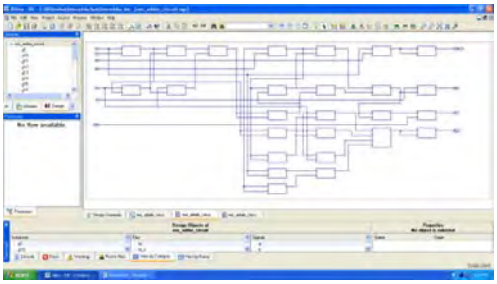


Figure.6 Internal Architecture of RBSD Adder Cell

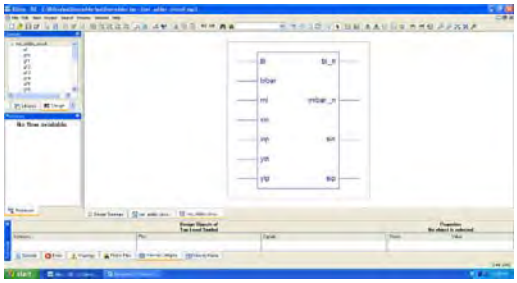


Figure.7 Block Diagram of RBSD(NOR-NOR) Adder Circuit

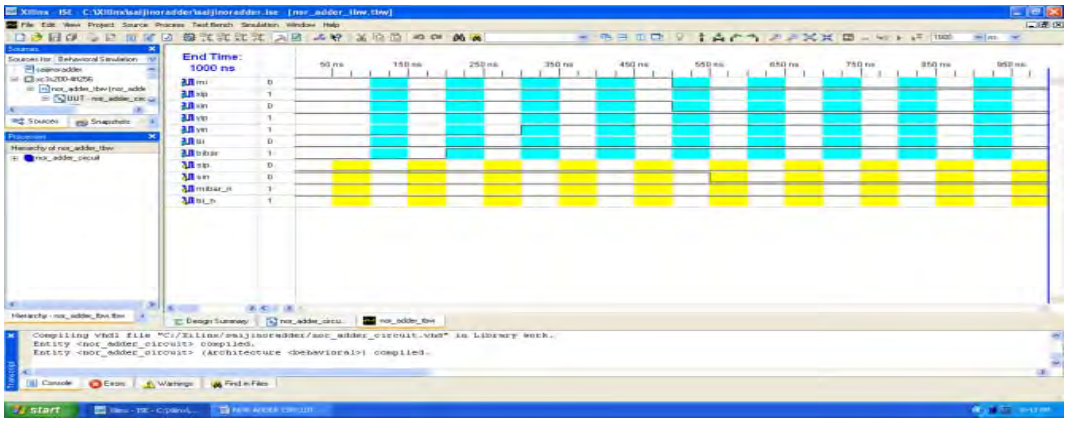
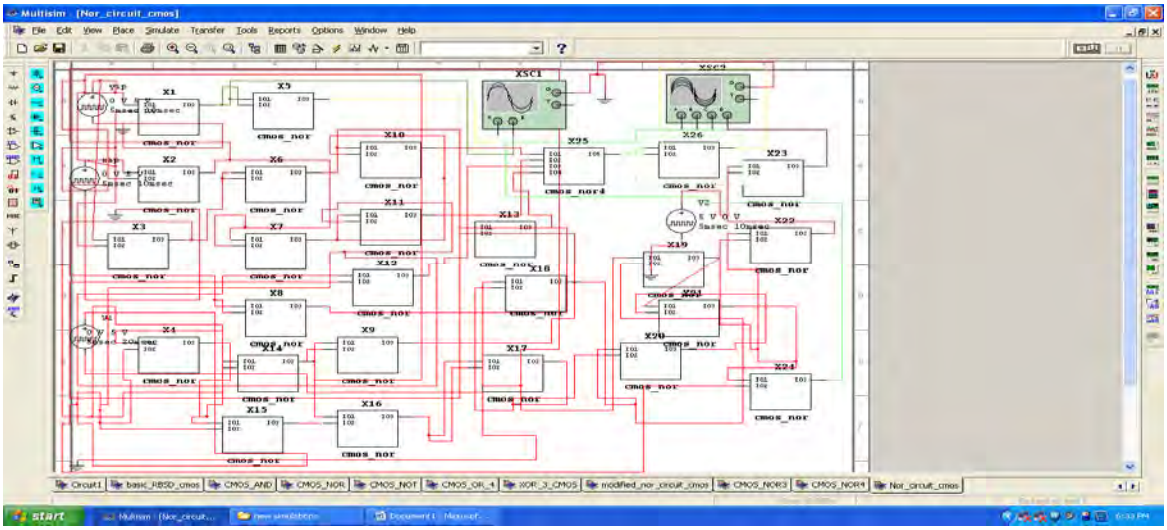


Figure.8 Simulation Result of RBSD Adder Cell(NOR-NOR)

FET Implementation of RBSD (NOR-NOR)Adder Cell



6. Comparison:

The path propagation delay and the peak memory used reports were generated using Xilinx Project Navigator and the comparison chart is shown in figure.

Type of RBSD Adder cell	Path Propogation Time Delay(ns)	Peak Memory Used(MB)
Basic RBSD	10.569	102
NOR-NOR	10.559	99

. Table 1: Comparative Analysis

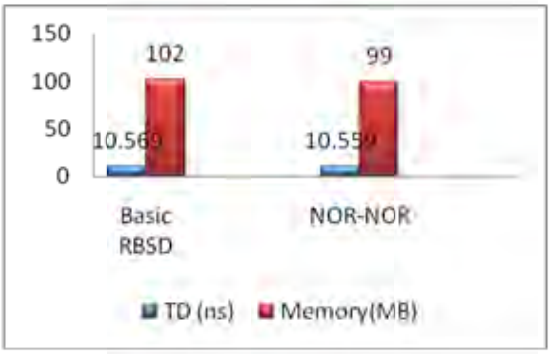


Figure 9:Graphical analysis of Basic RBSD and NOR-NOR Circuit

7. Conclusion:

It can be concluded from the table that the time of path delay for basic RBSD Cell proposed by Kal and Rajashekhar in 1990 is 10.569 ns and the peak memory used is 102 MB whereas the NOR-NOR Adder Circuit proposed by N.Sharma in 2006 has the delay of 10.559 ns and the memory used is 99 MB. Hence it is clear that the NOR-NOR circuit utilizes the memory space more efficiently and the delay is reduced.

References:

[1] Avizienis, A., "Signed digit number representation for fast parallel arithmetic", IRE Trans. Electron Computers., vol EC-10, pp. 389-400, sept.1961.
[2] Brent R. P., and Kung H. T., "A Regular Layout for Parallel Adders", IEEE Transactions on Computers, vol. C-24, no. 3, pp. 260-264, 1982.
[3] Hallin, T. G. and Flynn M. J., "Pipelining of Arithmetic Functions", IEEE Transactions of computers, pp. 880-885, 1972.
[4] Neelam Sharma, B. S. Rai and Arun Kumar, "Design of RBSD Adder and Multiplier Circuits for High Speed Arithmetic Operations and Their Timing Analysis", Special Russian Issue: Advances in computer Science and Engineering, Research in Computing Science23, pp. 243-25, 2006.
[5] Parhami B, "Carry free Addition of Recorded Binary Signed-Digit Numbers", IEEE Transactions on computers vol. 37 no. 11, pp. 1470-1476 ,1988.
[6] Perry D. L., VHDL Programming by Example, Tata McGraw – Hill Publishing Co. Ltd. Fourth Edition 2003.
[7] Rakesh Kumar Saxena, Neelam Sharma and A. K. wadhwani, "Fast Arithmetic using Signed Digit Numbers and Ternary Logic", Proceedings of Institute of American Physics, USA, vol. 1146, pp 488-498 July 2009.
[8] Rajashekhar, T.N.and Kal, O., "Fast Multiplier Design using Redundant Signed- Digit Numbers", International Journal of Electronics vol .69, no. 3, pp –359-368, 1990.
[9] Rajashekhar, T.N. and I-Shi Eric Chen, "A Fast Adder Design Using Signed-Digit Numbers and Ternary Logic", Proc. IEEE Southern Tier Technical Conference, pp.187-194, Binngamton, New York, April 1990.
[10] Rakesh Kumar Saxena, Neelam Sharma and A. K. Wadhwani "Novel Design of Fast RBSD Adder with Reduced NOR-NOR Logic "International Journal of Computer and Network Security,Vol. 2, No. 7, July \ 2010.