Low Power, Reduced Dynamic Voltage Swing Domino Logic Circuits

Salendra.Govindarajulu[1], Dr.T.Jayachandra Prasad[2], P.Rangappa[3]
[1]*Associate Professor, ECE, RGMCET, JNTU*
Email: rajulusg06@yahoo.co.in
[2]*Principal, RGMCET, JNTU*
[3]*P.G.Student, RGMCET*

***Abstract*— Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. In this work, new reduced – swing domino logic techniques which provide significant low power dissipation as compared to traditional domino circuit structures are proposed. The key idea of the new design styles is to limit both the upper and lower bounds of the voltage swing at the internal dynamic node. The voltage swing at the input and output of the circuits remains full – swing. The design styles are compared by performing detailed transistor level simulations on benchmark circuits such as OR2 gate, AND2 gate, XOR2 gate, 16-bit adder, 16-bit Comparator and 4-bit LFSR(Linear Feedback Shift Register) using Dsch3 and Microwind3 CAD tool.**

***Index Terms*—CMOS, Domino logic, Dynamic power, Full-swing, Low Power, Reduced-swing.**

I. INTRODUCTION

The power consumed in high performance microprocessors has increased to levels that impose a fundamental limitation to increasing performance and functionality [1]–[3]. If the current trend in increasing power continues, high performance microprocessors will soon consume thousands of watts. The power density of a high performance microprocessor will exceed the power density levels encountered in typical rocket nozzles within the next decade [2].

The generation, distribution, and dissipation of power are at the forefront of current problems faced by the integrated circuit industry [1]–[5]. The application of aggressive circuit design techniques which only focus on enhancing circuit speed without considering power is no longer an acceptable approach in most high complexity digital systems. Dynamic switching power, the dominant component of the total power consumed in current CMOS technologies, is quadratically reduced by lowering the supply voltage. Lowering the supply voltage, however, degrades circuit speed due to reduced transistor currents. Threshold voltages are scaled to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1]–[5]. At reduced threshold voltages, however, subthreshold leakage currents increase exponentially. Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [7]–[8]. However, deep sub micrometer (DSM) domino logic circuits utilizing low power supply and threshold voltages have decreased noise margins [9]–[11]. As on-chip noise becomes more severe with technology scaling and increasing operating frequencies, error free operation of domino logic circuits has become a major challenge [9], [10], [11].

The focus of this paper is to implement various Reduced-swing domino logic circuit techniques which offer better speed, energy-efficiency and noise immunity in DSM technology. The organization of the paper is as follows. A brief review of the sources of power dissipation in CMOS circuits is provided in Section II. In Section III various Reduced-swing techniques in domino logic circuits for power reduction are proposed. In Section IV simulation and implementation results are presented. Finally, conclusions are presented in Section V.

II. SOURCES OF POWER DISSIPATION

The power consumed by CMOS circuits can be classified into two categories:

A. Dynamic Power Dissipation

For a fraction of an instant during the operation of a circuit, both the PMOS and NMOS devices are "on" simultaneously. The duration of the interval depends on the input and output transition (rise and fall) times. During this time, a path exists between V_{dd} and G_{nd} and a short-circuit current flows. However, this is not the dominant factor in dynamic power dissipation. The major component of dynamic power dissipation arises from transient switching behavior of the nodes. Signals in CMOS devices transition back and forth between the two logic levels, resulting in the charging and discharging of parasitic capacitances in the circuit. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation.

B. Static Power Dissipation

This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The subthreshold leakage current increases exponentially, thereby increasing static power dissipation.

III. CIRCUIT TECHNIQUES

Dynamic domino logic circuits are widely used in modern VLSI circuits. These dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. This work discusses several domino circuit design techniques to reduce the power dissipation of domino logic while simultaneously improving noise immunity. The benefits are achieved by limiting the voltage swing of the internal dynamic node in a typical domino gate. This dynamic storage node is the node connected to the input of the output inverter of a domino gate as shown in fig.1. In a standard domino circuit the dynamic node is precharged to a high voltage level V_{dd}, then conditionally discharged to '0' voltage or ground during the evaluation phase. This work discusses circuits where the upper level of the dynamic node is reduced by the threshold voltage V_t, of an NMOS transistor where as the lower level of the voltage swing is increased to the threshold voltage V_{tp}, of a PMOS transistor. Specifically, the voltage swing of the dynamic node is between V_{tp} and V_{dd}-V_{tn}. A variety of circuit configurations to achieve such reduced – swing at the dynamic node of a domino gate are presented and analyzed.

Reduced Dynamic Swing Domino (RDS- Domino):

Reducing the voltage–swing at the dynamic node in the domino circuits has two objectives. First, the power dissipation of such a circuit will be lower since the capacitive load associated with the dynamic node is charged to a lower voltage level. Additionally, the reduced swing circuit will be more tolerant to noise because of the increased voltage level at the base of the pull down network (PDN). If the dynamic node is to be discharged to the threshold value rather than to ground, then the voltage level at the base of the PDN must necessarily be resting at the desired threshold value. Hence, a potentially hazardous noise spike must rise a threshold above this increased voltage level (V_{tn}+V_{tp}~2V_{tn}) to turn on the NMOS transistors in the PDN and begin discharging the dynamic node. In a traditional domino circuit such as shown in fig.1, a V_{tn} noise spike is sufficient to begin to turn on the NMOS transistors in the pull down network.

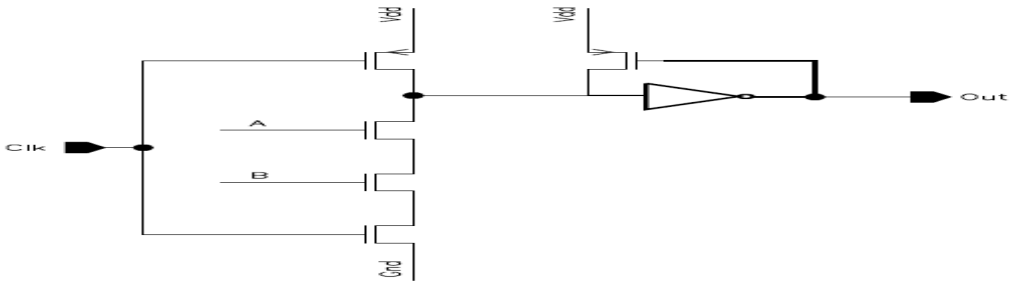

Fig.1. Standard domino logic structure

However, the increased voltage level (during evaluation phase) at the base of pull down network also leads to an increase in propagation delay since all input signals must reach the elevated signal level of ~$2V_{tn}$ in order for the dynamic node to begin discharging. A complete analysis of the effects of the reduced swing at the dynamic node on both noise tolerance and propagation delay is presented with respect to specific circuit configurations below.

A. Reduced–Swing Domino with Dual supply (RSDLS):

The first circuit configuration proposed to reduce the dynamic node voltage swing is obtained by simply altering the appropriate supply voltages of the standard domino gates as shown in fig.2.

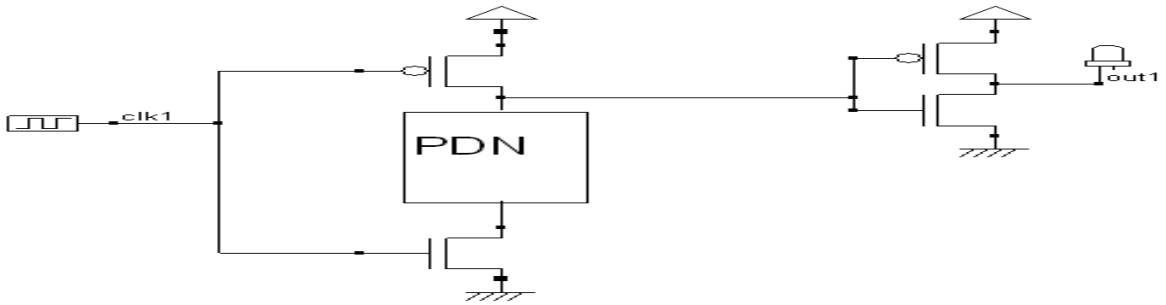

Fig.2. Reduced–Swing Domino with Dual Supply

This circuit is here after referred to as a reduced–swing (RSDLS) domino gate with dull supply. In a traditional domino circuit structure the voltage–swing at the dynamic node is ($V_{dd} - V_{ss}$). Here the upper bound on the voltage swing at the dynamic node is set to a level $V_{ddL} = (V_{dd} - V_{tp})$ and the lower level of the voltage swing is set to a level $V_{ssH} = (V_{ss} + V_{tn})$. The RSDLS domino gate operates exactly as a standard domino gate, except for the reduced–swing ($V_{dd} - V_{tp}$) – ($V_{ss} + V_{tn}$) at the dynamic node.

B. Reduced –Swing Domino with Single supply (RSSLS):

The *RSDLS* circuit shown above is simplified by replacing the extra supply voltages with transistors providing the desired threshold voltage drops. Two alternative configurations are proposed and are shown in fig.3 and fig.4. In fig.3 an NMOS transistor is inserted above the precharge transistor and a PMOS transistor is inserted beneath the footer. This arrangement provides reduced voltage swing at the dynamic node due to the threshold drop of the added transistors.

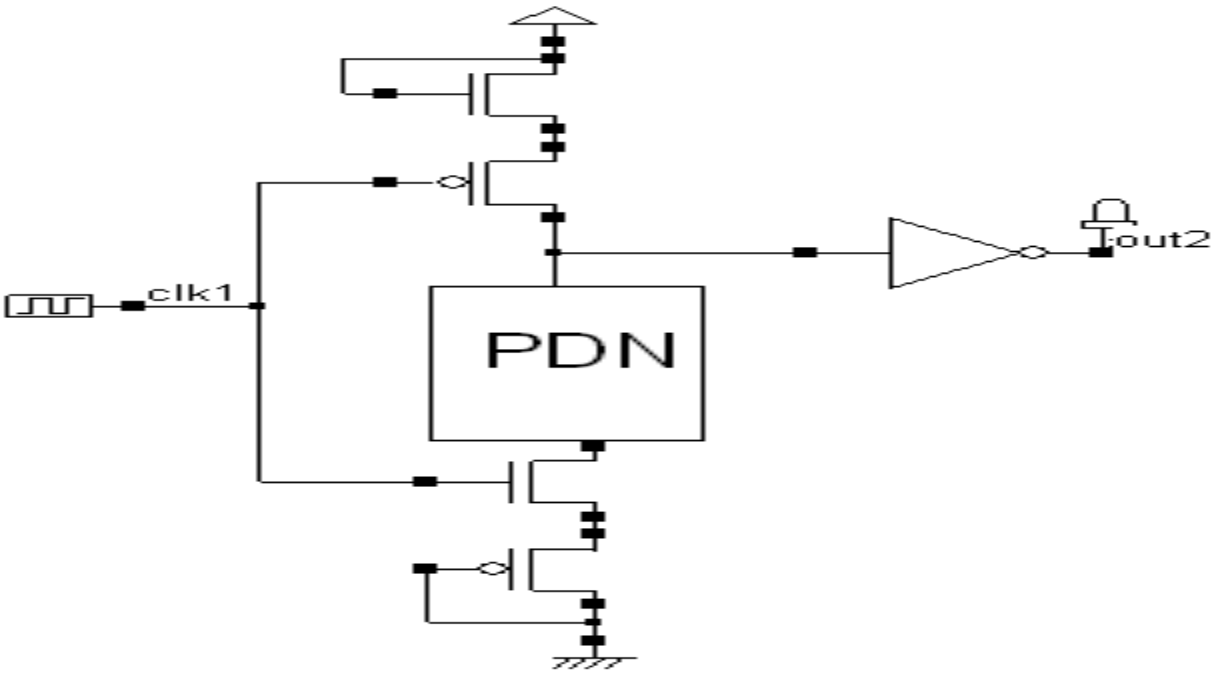

Fig.3. Reduced – Swing Domino with Single supply

C. Reduced Swing Mirror Domino (RSMRD):

This is one of the alternative approaches for having reduced swing, which is shown in fig.4. This is an arrangement in which the precharge and footer transistors are exchanged with an NMOS and PMOS transistor respectively. This circuit is referred to as reduced–swing mirror–domino (RSMRD) circuit, since the transistors have been reversed as if reflected across the dynamic node. This circuit is identical to standard domino circuit structure except for changing the types of these two transistors.

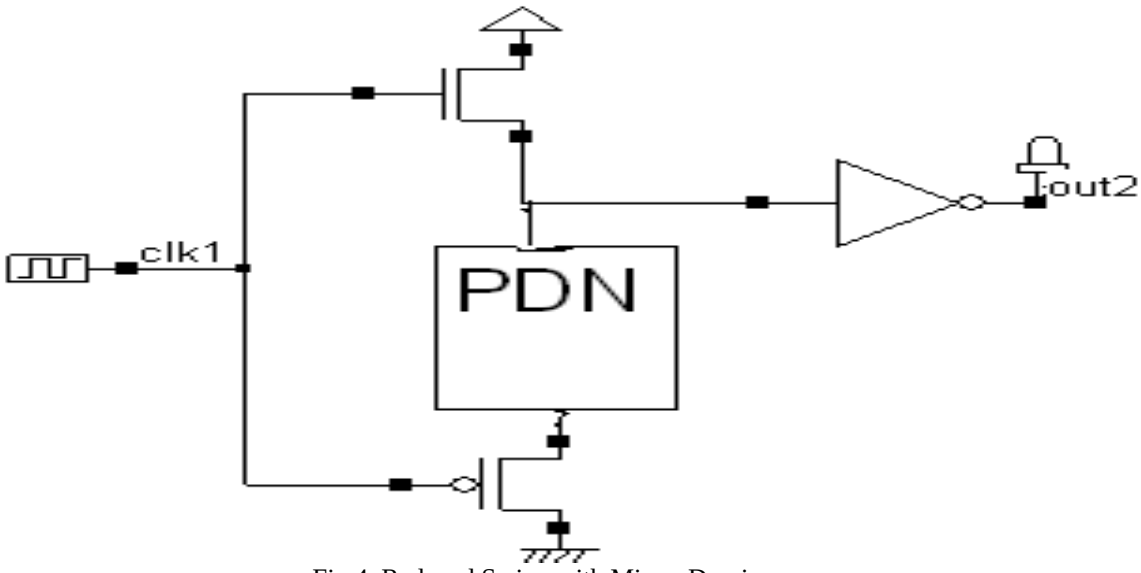

Fig.4. Reduced Swing with Mirror Domino

This arrangement dictates that the precharge and evaluate cycles be reversed with regard to clock. That is, clock begins high corresponding to precharge and clock goes low corresponding to the evaluate cycle. Given this

arrangement, the voltage swing of the internal dynamic node is limited by the transistor thresholds. The supply voltage and the input/ output signals all remain unmodified.

IV. SIMULATION AND IMPLEMENTATION RESULTS

In this work, the benchmark circuits using the stated four techniques are implemented. The figures of merits used to compare these techniques are power consumption, propagation delay and power delay product (PDP). The benchmark circuits implemented are OR2 gate, AND2 gate, XOR2 gate, 16-bit adder, 16-bit Comparator and 4-bit LFSR (Linear Feedback Shift Register). These design styles are compared by performing detailed transistor-level simulations on benchmark circuits using DSCH3 and Microwind3 CAD tool for 120 nm and 65 nm technology. The results of the benchmark circuits for all techniques are given below. Table1 shows the comparison of all the three proposed techniques with that of standard domino (std–domino) circuit for two input OR gate. Table2 shows the comparison of all the three proposed techniques with that of standard domino circuit for two input AND gate. Table3 shows the comparison of all the three proposed techniques with that of standard domino circuit for two input XOR gate. Table4 shows the comparison of all the three proposed techniques with that of standard domino circuit for 16-bit adder. Table5 shows the comparison of all the three proposed techniques with that of standard domino circuit for 16-bit Comparator. Table6 shows the comparison of all the three proposed techniques with that of standard domino circuit for 4-bit LFSR. From the results, it can be observed that the proposed logic techniques, viz., RSSLS, RSDLS and RSMRD domino logic techniques provide lower values of power dissipation, propagation delay and PDP when compared to the standard domino logic structure.

TABLE1. SHOWING VALUES OF POWER (μ Watts), DELAY (ns), AND PDP (*10^{-15} Watt-Sec) OF OR2 GATE:

Techniques		Power	Delay	Power Delay Product
RSDLS	65nm	0.007	0.051	0.000357
	120nm	15.891	0.038	0.603858
RSSLS	65nm	17.094	0.03	0.51282
	120nm	24.64	0.033	0.81312
RSMRD	65nm	0.0322	0.029	0.000933
	12nm	0.8	0.032	0.0256
Std-Domino	65nm	0.433	0.023	0.009959
	12nm	1.038	0.019	0.019722

TABLE2. SHOWING VALUES OF POWER (µ Watts), DELAY (ns), AND PDP (*10^{-15} Watt-Sec) OF AND2 GATE:

Techniques		Power	Delay	Power Delay Product
RSDLS	65nm	21.635	0.031	0.670685
	120nm	28.526	0.031	0.884306
RSSLS	65nm	32.102	0.051	1.637202
	120nm	27.618	0.028	0.77304
RSMRD	65nm	0.355	0.023	0.008165
	120nm	0.745	0.027	0.020115
Std-Domino	65nm	0.506	0.074	0.03744
	120nm	0.870	0.030	0.0261

TABLE3. SHOWING VALUES OF POWER (µ Watts), DELAY (ns), AND PDP (*10^{-15} Watt-Sec) OF XOR2 GATE:

TECHNIQUES		Power	Delay	Power Delay Product
RSDLS	65nm	22.881	0.038	0.869478
	120nm	10.282	0.037	0.380434
RSSLS	65nm	23.002	0.033	0.759066
	120nm	22.903	0.036	0.824508
RSMRD	65nm	1.592	0.03	0.04776
	12nm	3.476	0.033	0.114708
Std-Domino	65nm	1.711	0.025	0.042775
	12nm	3.74	0.02	0.0748

TABLE4. SHOWING VALUES OF POWER (m Watts), DELAY (ns), AND PDP (*10^{-12}Watt-Sec) OF 16 BIT ADDER:

Techniques		Power	Delay	Power Delay Product
RSDLS	65nm	0.15	0.025	0.00375
	120nm	0.146	0.038	0.005548
RSSLS	65nm	0.649	0.015	0.009735
	120nm	0.134	0.109	0.014606
RSMRD	65nm	1.909	0.02	0.03818
	120nm	0.61	0.031	0.01891
Std-Domino	65nm	0.586	0.026	0.015236
	120nm	1.22	0.049	0.05978

TABLE5. SHOWING VALUES OF POWER (m Watts), DELAY (ns), AND PDP (*10^{-12}Watt-Sec) OF 16 BIT COMPARATOR:

Techniques		Power	Delay	Power Delay Product
RSDLS	65nm	1.053	0.069	0.072657
RSSLS	65nm	1.07	0.058	0.06206
RSMRD	65nm	6.901	0.041	0.282941
Std-Domino	65nm	0.833	0.033	0.027489

TABLE6. SHOWING VALUES OF POWER (m Watts), DELAY (ns), AND PDP (*10^{-12}Watt-Sec) OF 4- BIT LFSR:

Techniques		Power	Delay	Power Delay Product
RSDLS	65nm	0.024423	0.039	0.000952
RSSLS	65nm	0.683	0.027	0.018441
RSMRD	65nm	0.293	0.017	0.004981
Std-Domino	65nm	1.455	0.018	0.02619

V.CONCLUSIONS

In this work, an attempt has been made to simulate AND, OR, XOR gates, 16-bit adder, 16-bit Comparator and 4-bit LFSR by using the three proposed techniques. The proposed circuits have offered an improved performance in power dissipation, speed and noise tolerance when compared with standard domino circuit. As it is observed from the results, of all the three reduced swing circuits, reduced swing domino with dual supply has low power dissipation, PDP and more tolerance to noise. Therefore the proposed techniques offer better solution for the optimization of sub-threshold leakage and minimizing the overall power consumption of the domino circuit. Hence, it is concluded that the proposed designs will provide a platform for designing high performance and low power digital circuits such as, processors and multipliers.

ACKNOWLEDGMENT

The authors wish to thank RGMCET, Nandyal, A.P, India for providing the Microwind3 and DSCH tools.

REFERENCES

[1] S. Borkar, “Obeying moore’s law beyond 0.18 micron,” in Proc. IEEE Int. ASIC/SOC Conf., Sept.2000, pp. 26–31.
[2] R. Ronen et al., “Coming challenges in microarchitecture and architecture,”Proc. IEEE, vol. 89, pp. 325–339, Mar. 2001.
[3] M. T. Bohr, “Nanotechnology goals and Challenges for electronic applications,”IEEE Trans.Nanotechnol., vol. 1, pp. 56–62, Mar. 2002.
[4] D. J. Frank et al., “Device scaling limits of Si MOSFET’s and their application dependencies,” Proc. IEEE, vol. 89, pp. 259–288, Mar. 2001.
[5] R. K. Krishnamurty, A. Alvandpour, V. De, and S. Borkar, “High-performance and low-power challenges for sub-70 nm microprocessor circuits,”in Proc. IEEE Custom Integrated Circuits Conf., May 2002, pp.125–128.
[6] S. Mutoh et al., “1-V power supply high-speed Digital circuit technology with multithreshold- voltage CMOS,” IEEE J. Solid-State Circuits, vol.30, pp. 847–854, Aug. 1995.
[7] V. Kursun and E. G. Friedman, “Domino logic with dynamic body Biased keeper,” in Proc. Eur. Solid-State Circuits Conf., Sept. 2002, pp.675–678.
[8] “Variable threshold voltage keeper for contention reduction in dynamic circuits,” in Proc. IEEE Int. ASIC/SOC Conf., Sept. 2002, pp.314–318.
[9] S. Borkar, .Low Power Design Challenges for the Decade,. Proceedings of the IEEE/ACM Design Automation Conference, pp. 293-296, June 2001.
[10] P. Srivastava, A. Pua, and L. Welch, .Issues in the Design of Domino Logic Circuits,. Proceedings of the IEEE Great Lakes Symposium on VLSI, pp. 108-112, February 1998.
[11] G. Balamurugan and N. R. Shanbhag, .Energy- efficient Dynamic Circuit Design in the Presence Crosstal Noise,. Proceedings of the IEEE International Symposium on Low Power Electronics and Design, pp. 24-29, August 1999.
[12] Salendra.Govindarajulu, Dr.T.Jayachandra Prasad “Considerations of Performance Factors in CMOS Designs,” in Proc. of 2008 International Conference in Electronic Design, IEEE , December 1-3, 2008,Penang, Malaysia.
[13] Salendra.Govindarajulu, Dr.T.Jayachandra Prasad “Low Power, Energy-efficient Domino logic Circuits,” CEE2009, IJRTE, Volume 2, Number 7, November 2009,pp.30-33 Academy Publishers, Finland .

Biographical Notes

[1]Salendra.Govindarajulu:- He is working as an Associate Professor in the Dept. of Electronics & Communication Engg. at RGMCET, Nandyal, Andhra Pradesh, India. He presented more than 16 International/National Technical Papers. He is a Life Member of ISTE, New Delhi. His Research interest includes Low Power VLSI CMOS design.

[2]Dr.T.Jayachandra Prasad:- He is working as a Principal and Professor in the Dept. of Electronics & Communication Engg. at RGMCET, Nandyal, Andhra Pradesh, India. He presented more than 42 International/National Technical Papers. He is Life Member in IE (I), CALCUTTA, Life Member in ISTE, NEW DELHI, Life Member in NAFEN, NEW DELHI, and IEEE Member. His interest includes Digital Signal Processing.